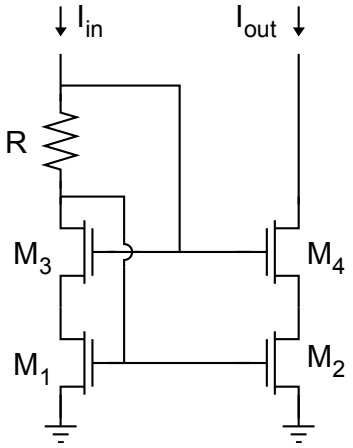
EE 551 Linear Integrated Circuits
Homework 5

Unless otherwise specified, use the following transistor parameters.

$V_{T0} = 0.7V$, $\gamma = 0.4V^{1/2}$, $\varphi_F = 0.35V$, $\kappa_n = \kappa_p = 0.65$ (subthreshold), $\mu_n=1360cm^2/Vs$, $\mu_p=460cm^2/Vs$, $K' = 100\mu A/V^2$, $I_0 = 1pA$, $I_{th} = 1\mu A$, $V_A = 50V$, $K_s=11.8$, $\varepsilon_0=8.854x10^{-12}F/m$, $T=300K$, $V_{dd} = 5V$, $V_{bi} = 0.7V$, $m=1$

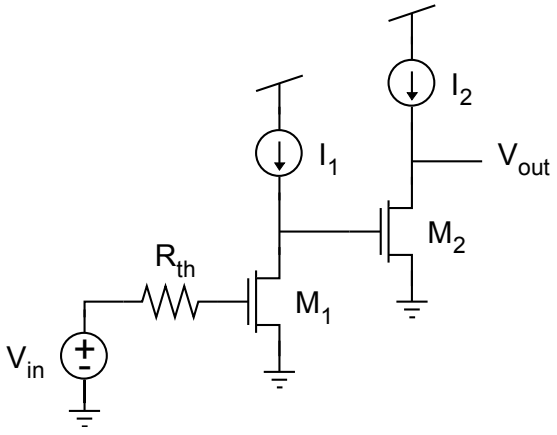
1. For the following circuit, design the current mirror (W/L ratios and R) for a current of $I_{in} = I_{out} = 100\mu A$ and $V_{out,min} = 0.4V$. Let all transistors be of equal size.



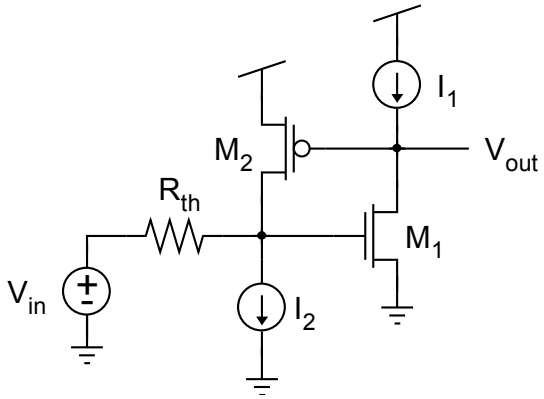
2. An nFET is biased such that the source is at 1V and the drain is at 2V. The size of the transistor is W = 100μm and L = 1μm. The overlap capacitance is Cov = 0.1fF/μm, the oxide capacitance is Cox = 3.5fF/μm^2, and the diffusion region depletion capacitances (zero-bias) are $C_{sb0} = C_{db0} = 100fF$ (incorporates C_{j0}, C_{jsw0}, and the areas of the diffusion regions). Determine the complete small signal model (transconductances, resistances, and capacitances) and the unity-gain frequency (f_T) for the following conditions.
   a. $I_D = 500\mu A$
   b. $I_D = 10nA$

3. Use the Miller Effect to estimate expressions for all three poles for a cascaded common-source amplifier with a resistive load. Explain why a cascade improves the maximum frequency of operation.

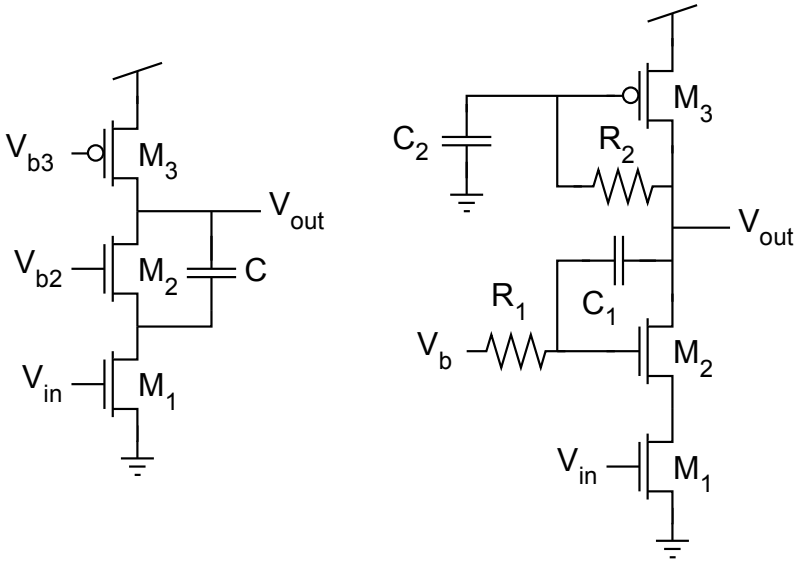
4. Use the Miller Theorem to determine all poles in the following circuit.



5. Determine the transfer function of the following circuit including all parasitic capacitances.



6. Find the gain at very-low frequencies and at very-high frequencies for the following circuits.



(a) (b)