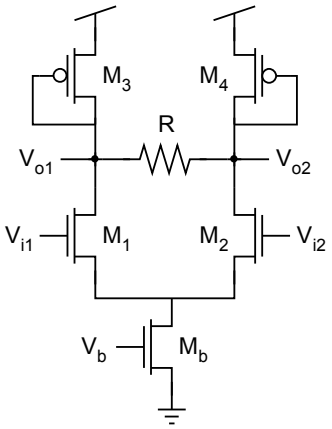
EE 551 Linear Integrated Circuits
Homework 6

Unless otherwise specified, use the following transistor parameters.

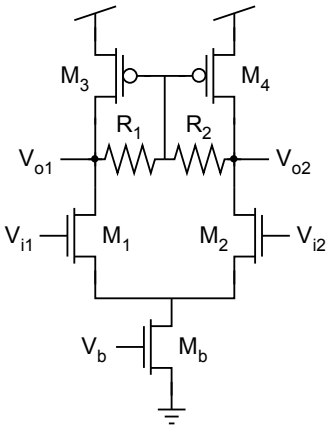
$V_{T0} = 0.7V$, $\gamma = 0.4V^{1/2}$, $\varphi_F = 0.35V$, $\kappa_n = \kappa_p = 0.65$ (subthreshold), $\mu_n=1360cm^2/Vs$, $\mu_p=460cm^2/Vs$, $K' = 100\mu A/V^2$, $I_0 = 1pA$, $I_0' = 0.1pA$, $I_{th} = 1\mu A$, $V_A = 50V$, $K_s=11.8$, $\varepsilon_0=8.854x10^{-12}F/m$, $T=300K$, $V_{dd} = 5V$, $V_{bi} = 0.7V$,

1. For an nFET-based differential paire, answer the following questions. Assume that the input pair have W/L = 50µm/0.5µm, I_b = 1mA, and that $\lambda = 0$.
   a. What is the overdrive voltage of each transistor if $V_{in} = 0$?
   b. How is the bias current shared between the two input transistors if V_{in} = 50mV?
   c. For $I_{out} = I_1 - I_2$ and V_{in} = 50mV, what is the effective transconductance of the differential pair? Assume that this input voltage is within the linear range of the circuit.

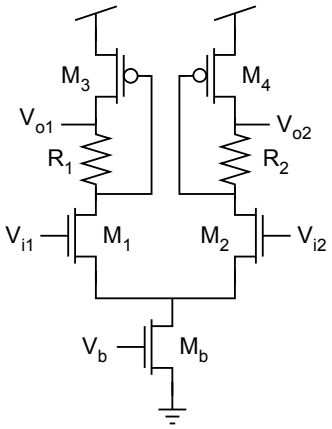
2. Calculate expressions for the small-signal differential voltage gain of each of the following circuits.



(a)

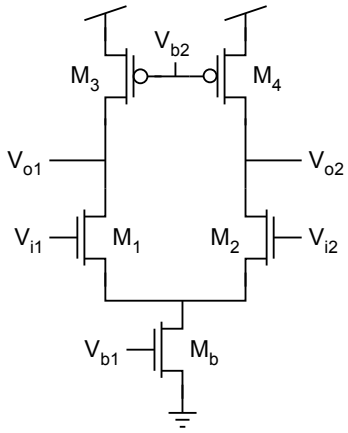


(b)



(c)

3. For the following circuit, determine the following. Assume that M1-4 have W/L ratios of 50µm/0.5µm, Ib = 1mA, and $\gamma = 0$.



   a. Determine the small-signal differential voltage gain.
   b. Determine the maximum allowable output voltage swing of $V_{in,cm}$ = 1.5V.

4. Calculate the following parameters given that I_{b1} = 100nA, C_L = 1pF, $M_{1\text{-}10}$ and M_{b1} have W/L ratios of 10µm/1µm, and $M_{b2\text{-}5}$ are appropriately sized to set the bias voltages for M_9 and M_{10} and have 50nA flowing through them.
   a. Calculate the output resistance.
   b. Calculate the small-signal differential voltage gain.
   c. Calculate the slew rate.
   d. Calculate the power dissipation.
   e. Calculate the gain-bandwidth product, assuming that the output pole is the dominant pole.
   f. Design the sizes of $M_{b2\text{-}5}$ to appropriately bias transistors M_9 and M_{10}.