For an nFET based differential pair with input transistors that are $W/L = 50/0.5$ μm and a bias current of 1mA, (let $\lambda = 0$)

a) What is the overdrive voltage of each transistor? (Let $V_{in} = 0$)

$$I = \frac{K'\frac{W}{L}}{2}\underbrace{(V_{gs} - V_T)}_{V_{ov}}^2$$

at $V_{in} = 0$, $I_1 = \frac{1}{2} I_b = I_2$

$$V_{ov} = \sqrt{\frac{2I}{K'\frac{W}{L}}} = \sqrt{\frac{2(0.5mA)}{(100\,\mu A/V^2)(100)}} = \sqrt{0.1V^2} = \boxed{0.3162\ V}$$

b) How is the bias current shared between the two input transistors if $V_{in} = 50mV$?

$$I_1 = \frac{I_b}{2} + \frac{K'\frac{W}{L}}{4} V_{in}\sqrt{\frac{4I_b}{K'\frac{W}{L}} - V_{in}^2}$$

$$= 0.5mA + \frac{0.01\ A/V^2}{4}(50mV)\sqrt{\frac{(4)(1mA)}{0.01\ A/V^2} - (50mV)^2} =$$

$$= 0.5788\ mA$$

$$I_2 = \frac{I_b}{2} - \frac{K}{4} V_{in}\sqrt{\frac{4I_b}{K} - V_{in}^2} = 0.4212\ mA$$

c) For $I_{out} = I_1 - I_2$ and $V_{in} = 50mV$ (assume this is in the linear range), determine the effective transconductance of the differential pair

$$I_{out} = I_1 - I_2 = \frac{K}{2} V_{in}\sqrt{\frac{4I_b}{K} - V_{in}^2}$$

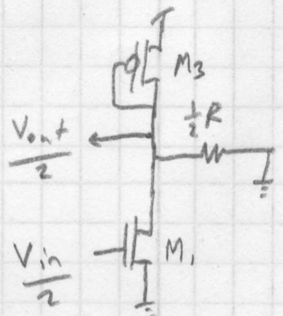
$$G_m = \frac{\partial I_{out}}{\partial V_{in}} = \frac{K}{2}\sqrt{\frac{4I_b}{K} - V_{in}^2} + \frac{\frac{1}{2}\left(\frac{K}{2}V_{in}\right)(-2V_{in})}{\sqrt{\frac{4I_b}{K} - V_{in}^2}} =$$

$$= \frac{K}{2}\,\frac{\frac{4I_b}{K} - V_{in}^2 - V_{in}^2}{\sqrt{\frac{4I_b}{K} - V_{in}^2}} = \frac{K}{2}\,\frac{\frac{4I_b}{K} - 2V_{in}^2}{\sqrt{\frac{4I_b}{K} - V_{in}^2}} =$$

$$= 3.1227\ mS$$

Calculate the small-signal differential voltage gain for the following circuits

a) We can use the differential half circuit for each of these three parts



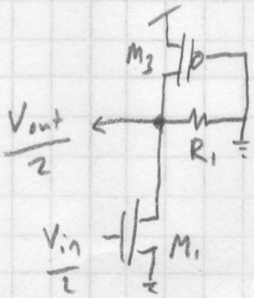
$$a_v = -g_{m1}\ r_{o1} \| r_{o3} \| \tfrac{1}{2}R \| \frac{1}{g_{m3}}$$

$$\frac{1}{g_{m3}} \ll r_{o1},\ r_{o3}$$

we don't know what R is

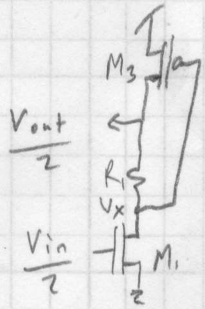
$$\therefore\ a_v \approx -g_{m1}\left(\frac{1}{g_{m3}} \| \frac{R}{2}\right)$$

b)

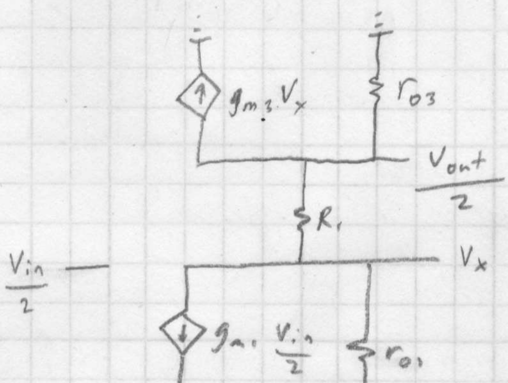


$$a_v = -g_{m1}\ r_{o1} \| r_{o3} \| R_1$$

c)



$\Rightarrow$



KCL at $V_x \rightarrow \frac{1}{2} g_{m1} v_{in} + \frac{V_x}{r_{o1}} + \frac{V_x - \frac{V_{out}}{2}}{R_1} = 0 \Rightarrow \frac{1}{2} g_{m1} v_{in} + \underbrace{V_x\left(\frac{1}{r_{o1}} + \frac{1}{R_1}\right)}_{\frac{V_x(R_1 + r_{o1})}{r_{o1} R_1}} = \frac{V_{out}}{2R_1}$

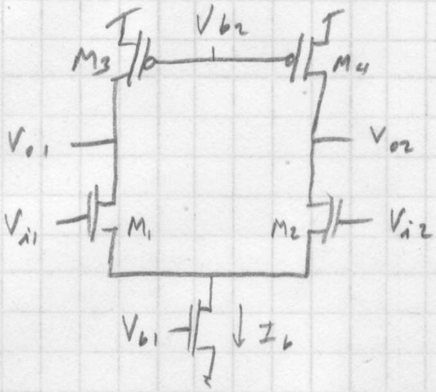
KCL at $\frac{V_{out}}{2} \rightarrow g_{m3} V_x + \frac{1}{2}\frac{V_{out}}{r_{o3}} + \frac{\frac{1}{2}V_{out} - V_x}{R_1} = 0$

$$V_x = \frac{\frac{1}{2} V_{out}\left(\frac{1}{r_{o3}} + \frac{1}{R_1}\right)}{\frac{1}{R_1} - g_{m3}} = \frac{V_{out}(R_1 + r_{o3})}{2 r_{o3}(1 - R_1 g_{m3})}$$

$$\cancel{\tfrac{1}{2}} g_{m1} v_{in} = \cancel{\tfrac{1}{2}} V_{out}\left[\frac{1}{R_1} - \frac{(R_1 + r_{o3})(R_1 + r_{o1})}{(r_{o1} r_{o3} R_1)(1 - R_1 g_{m3})}\right] = V_{out}\left[\frac{\cancel{r_{o1} r_{o3}} - r_{o1} r_{o3} \cancel{R_1} g_{m3} - \cancel{R_1}(r_{o1} + r_{o3} + R_1) - \cancel{r_{o1} r_{o3}}}{r_{o1} r_{o3} \cancel{R_1}(1 - R_1 g_{m3})}\right]$$

$$a_v = \frac{v_{out}}{v_{in}} = \frac{-g_{m1} r_{o1} r_{o3}(1 - R_1 g_{m3})}{r_{o1} + r_{o3} + R_1 + r_{o1} r_{o3} g_{m3}}$$

Calculate the voltage gain of the following circuit — Let $\gamma = 0$



Let $\left.\frac{W}{L}\right|_{1-4} = \frac{50\mu m}{0.5\mu m} = 100$

$I_b = 1mA$

$a_v = g_{m1} r_{o1} \parallel r_{o3}$

$r_{o1} = r_{o3} = \frac{V_A}{\frac{1}{2}I_b} = \frac{50V}{0.5mA} = 100k\Omega$

$g_{m1} = \sqrt{2K\frac{1}{2}I_b} = \sqrt{KI_b} = \sqrt{(100\mu A/V^2)(1mA)(100)} = 3.162mS$

$\therefore a_v = -g_{m1} r_{o1} \parallel r_{o3} = -(3.162mS)\left[100k\Omega \parallel 100k\Omega\right] = -158.114$

Find the maximum allowable output voltage swing if $V_{in,cm} = 1.5V$

Maximum $\rightarrow V_{dd} - V_{ov3}$ $\quad V_{ov3} = \sqrt{\frac{2I}{K}} = \sqrt{\frac{(1mA)}{(100\mu A/V^2)(100)}} = 0.3162V$

$\hookrightarrow 5 - 0.3162V = 4.6838V$

$2\frac{1}{2}I_b = I_b$

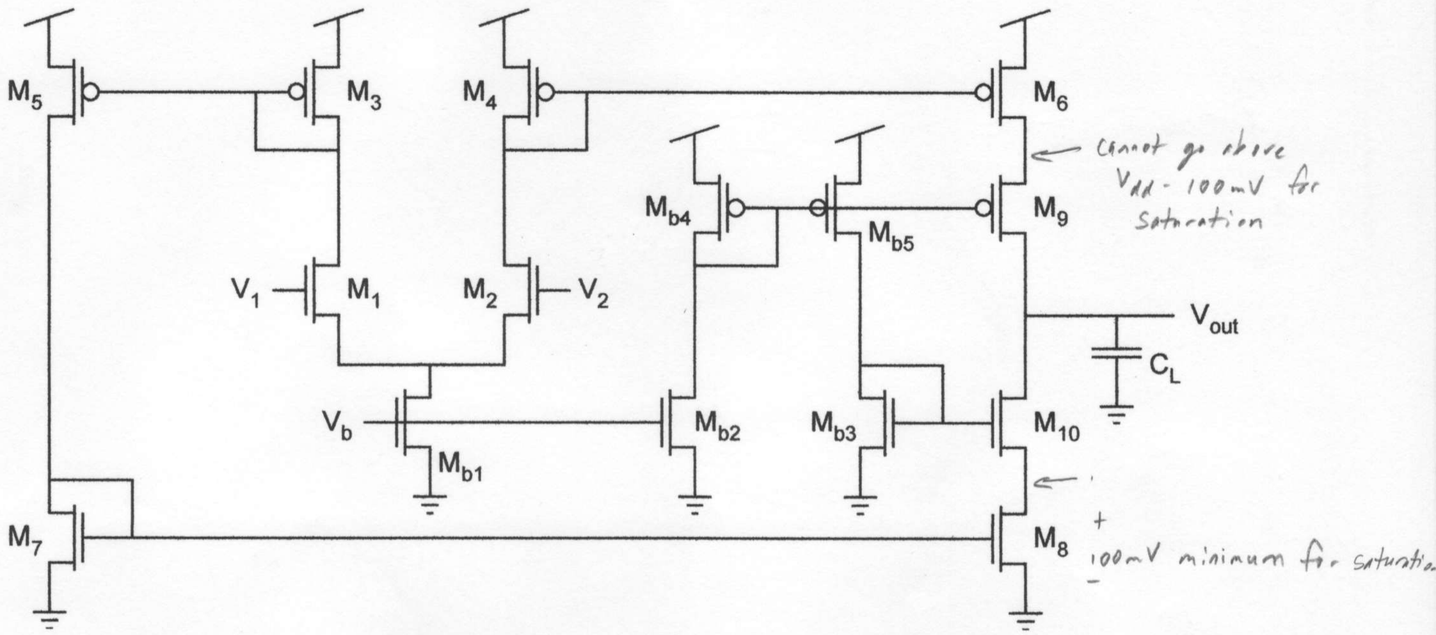
Minimum $\rightarrow V_{dd} - V_{sat3} - V_{sat1} + V_{gs1}$

$V_{in,cm} = V_{gs1} + V_{sat,b}$

$\therefore V_{in,cm} - V_{T1} = 1.5V - 0.7V = 0.8V$

Calculate the following parameters given that I_{b1} = 100nA, C_L = 1pF, $M_{1\text{-}10}$ and M_{b1} have W/L ratios of 10µm/1µm, and $M_{b2\text{-}5}$ are appropriately sized to set the bias voltages for M_9 and M_{10} and have 50nA flowing through them.

a. Calculate the output resistance.
b. Calculate the small-signal differential voltage gain.
c. Calculate the slew rate.
d. Calculate the power dissipation.
e. Calculate the gain-bandwidth product, assuming that the output pole is the dominant pole.
f. Design the sizes of $M_{b2\text{-}5}$ to appropriately bias transistors M_9 and M_{10}.



$R_{out} = r_{o6}\, g_{x9}\, r_{o9} \,//\, r_{o9}\, g_{x10}\, r_{o10}$ $\quad g_{x9} = g_{x10} = |g_{s9}| = \frac{I_9}{U_T} = \frac{50nA}{25.9mV} = 1.93\mu S$

$r_{o6} = r_{o8} = r_{o9} = r_{o10} = \frac{V_A}{I_b} = \frac{50V}{50nA} = 1\ G\Omega$

$R_{out} = \frac{1}{2} r_{o6}\, g_{x9}\, r_{o9} = \left(\frac{1}{2}\right)(1G\Omega)(1.93\mu S)(1G\Omega) = \boxed{965\ G\Omega}$

$a_v = -g_{m1} R_{out}$ $\quad g_{m1} = \frac{\kappa I_1}{U_T} = \frac{(0.65)(50nA)}{25.9mV} = 1.25\mu S$

$\therefore a_v = -(1.25\mu S)(965G\Omega) = \boxed{-1.2\times10^6}$

$SR = \frac{I_b}{C_L} = \frac{100nA}{1pF} = 100\ kV/s = \boxed{0.1\ V/\mu s}$

$P_{diss} = (100nA)V_{dd} + (4)(50nA)V_{dd} = 1.5\mu W$ ← Must account for current through each branch (going to ground)

$GB = \frac{g_{m1}}{C_L} = \frac{g_{m1} R_{out}}{R_{out} C_L} = \frac{1.25\mu S}{1pF} = 1.25\ MHz$

Design of M_{b2-5}

For M_{10} → V_{s10} cannot go below 100 mV

$$\therefore \quad I_{10} = I_o e^{\kappa V_{g10}/U_T} e^{-V_{s10}/U_T}$$

← with $V_A = 50V$, the Early voltage will have minimal impact here

$$\ln\left(\frac{I_{10}}{I_o}\right) = \frac{\kappa V_{g10} - V_{s10}}{U_T}$$

(V_{s10} → 100 mV)

$$\therefore V_{g10} = \frac{1}{\kappa}\left[U_T \ln\left(\frac{I_{10}}{I_o}\right) + V_{s10}\right] = \frac{1}{0.65}\left[25.9\,mV \ln\frac{50\,nA}{(0.1\,pA)(10)} + 0.100\,V\right]$$

(10 → $\frac{W}{L}$)

$$= 0.5850\,V$$

$V_{gb3} = V_{g10} = 0.5850V$ → Need to determine $\frac{W}{L}$ to achieve this voltage with 50 nA

$$I_{b3} = I_o e^{\kappa V_{gb3}/U_T} = I_o' \frac{W}{L} e^{\kappa V_{gb3}/U_T}$$

$$\frac{W}{L} = \frac{I_{b3}}{I_o' e^{\kappa V_{gb3}/U_T}} = \frac{50\,nA}{0.1\,pA\; e^{\kappa V_{gb3}/U_T}} = 0.21$$

Use reasonable sizes for W + L (e.g. 0.5 μm process)

Let $L_{b3} = 4.8\,\mu m$ → $W_{b3} = 1\,\mu m$

Let $M_{b4} = M_{b5}$ → 1:1 current mirror

Similar Design Procedure to above

V_{s9} cannot go above $V_{dd} - 100\,mV$

With the same parameters and biasing conditions as for M_{10}
→ will be the same values

Let $L_{b4} = L_{b5} = 4.8\,\mu m$, $W_{b4} = W_{b5} = 1\,\mu m$

Finally M_{b2} → must have half the current as is flowing through M_{b1} with the same bias voltage

$$\therefore W_{b2} = \frac{1}{2} W_{b1} = 5\,\mu m$$

$$L_{b2} = L_{b1} = 1\,\mu m$$