EE 551 Linear Integrated Circuits
Project 5
Single-Stage Amplifiers
35 Points

Objective
To learn how to simulate circuits with Cadence design tools and to understand the operation of simple single-stage amplifiers.

Special Directions
For this project, you do not need to turn in a paper copy of your report (electronic copy only). Feel free to turn in a paper copy, but depending on how you include your figures (i.e., simulation results), they may come out all black, and we don't need to waste a lot of toner.

Part 0 – Cadence Simulation Tutorials (0 Points)
Detailed instructions on how to use Cadence are provided on the class website at

http://community.wvu.edu/~dwgraham/classes/ee551/cad/cadence.html

This will be the first (of many) times that you will use Cadence in this class, so please take the time it requires to get really comfortable using these tools – it will only help you in the long run.

The above webpage has approximately 2.5 hours of video tutorials on how to use the Cadence suite of design tools. For this project, you will need to view only a portion of these tutorials. Please follow the instructions on the website very carefully. You are strongly encouraged to use the computers within the LCSEE computer labs. If you do not have an LCSEE username/account, please contact me immediately so that I can sponsor an account for you.

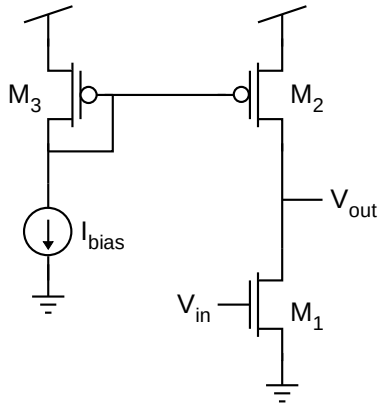
For this project, you are encouraged to go through Tutorials 1.1 – 3.6. At the barest minimum, you *must* go through Tutorials 1.1, 2.1, 3.1, and 3.4. Again, I strongly encourage you to go through all of Tutorials 1.1 – 3.6 since they will definitely help you both on this project and on future projects, as well. (Tutorials 4.1 – 6.1 will be covered later in the semester.)

These tutorials will describe how to create schematics within the Cadence environment, as well as how to run simulations. While many of you have used PSPICE in the past for circuit simulations, we will be using Spectre, which is Cadence's simulator. This simulator is much nicer in many ways, and it does not have the same constrictive limitations that PSPICE has (in terms of number of nodes and numbers of transistors). We will again make use of the Cadence tools for the physical design of integrated circuits later in the semester.

The tutorials show you how to incorporate simulation models in your design. These are BSIM models (not EKV). We will use BSIM in this project.

Part 1 – Common-Source Amplifier (25 Points)
You are to design a common-source (CS) amplifier under two specific situations – (1) a CS amplifier with a gain of 50 and (2) a CS amplifier with a gain of 300. Your gain needs to meet the required specification within 5% tolerance.

You should use the following schematic in your simulations to create the CS amplifier and properly bias it. In order to meet the gain specifications, you have several different parameters that you can adjust, such as the transistor sizes (W and L) and the bias current. Note that the pFET current mirror is used to appropriately bias the amplifier. In your report, you must specify the transistor sizes and the bias currents that provide the required gains (and putting these in a table form would be helpful).



You must demonstrate the gain in two different ways – through a DC sweep and through a transient analysis.

For the DC sweep, you should set up a DC simulation in which you sweep the input DC voltage. Indicate where the amplification region is, and also show what the gain of the circuit is. A few helpful suggestions are as follows.

- Make sure that your sweep is "dense" enough (i.e., that your step size is small enough to adequately capture the amplification region).
- The "calculator" function in the plot window is very, very useful. For instance, the derivative function in the calculator can be used to show the slopes in the plot – which could come in handy for this portion of the project.

For the transient sweep, you need to replace your input DC voltage source with a sinusoidal input source. You will also need to run a transient analysis instead of a DC analysis. You should use a relatively low-frequency signal, such as 100Hz. Make sure that you simulate long enough to observe a few periods of your waveform. A few helpful suggestions are as follows.

- Your input signal needs to be very small – small enough to fit within the "input linear range" of the amplifier (which is essentially the width of the amplification region on the x-axis of your DC plot. *State what size input signal you are using*. You must make sure that your output signal has no observable distortion (e.g., "clipping") – basically, the output should be a sinusoidal waveform at the same frequency, simply amplified in value, and it should look like a sinusoidal waveform.
- You need to carefully place the DC offset of your input signal to be exactly in the amplification region of your amplifier. Use your DC plots to help you determine where this location should be. *State in your report what your DC offset is.*

You should focus your report not only on the results but also the *methodology of how you approached the design*. State very clearly how you pursued achieving the desired gain. For example, how did you go about choosing transistor sizes, etc.?

Part 2 – Thought Questions (5 Points)

1. When looking at the DC sweeps off the CS amplifier for the two different gain values (50 and 300), you should note that the *shape* of the transfer function (Vout vs. Vin) is different for the two cases. Besides the fact that the slope in the amplification region is different (which is simply because the gain is different), describe two ways in which the shapes differ. Also, give a reason for what causes those two differences in the shapes. (4 Points)
2. What happens if your input DC offset shifts slightly – for example by 1mV or by 10mV? (1 Point)

Quality of Report (5 Points)

Please make sure that all numbers are readable, that the figures are large enough, and that there are no gross errors in terms of grammar, spelling or punctuation.