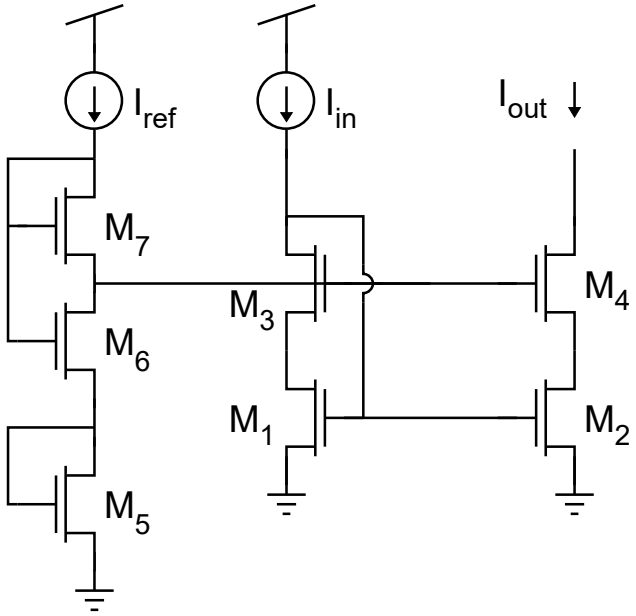
EE 551 Linear Integrated Circuits
Project 6
Advanced Current Mirror Design
55 Points

Objective
To learn how to use computer-aided design tools to design integrated circuits, and to understand the usage and implementation of cascoded circuits.

Special Directions
For this project, you do not need to turn in a paper copy of your report (electronic copy only). Feel free to turn in a paper copy, but depending on how you include your figures (i.e. simulation results), they may come out all black, and we don't need to waste lots of toner.

Part 1 – Current Mirror Design (50 Points)
Use Cadence to design the following current mirror.



For this design, use a supply voltage of V_{dd} = 3.3V. Your design must achieve the following specifications:

- $V_{out,min} \leq 0.425V$ (i.e. all transistors must be in saturation at this voltage)
- $I_{in} = 10\mu A$
- $I_{out} = 10\mu A$
- I_{out} must be within 0.1% of 10μA from 0.425V through 3.3V (i.e., $9.99\mu A \leq I_{out} \leq 10.01\mu A$)
- $I_{ref} = 100\mu A$ (this is the reference current to help generate your cascode bias voltage)

For your project report, give a ***detailed*** description of ***how*** you approached the design of this current mirror. Explain all the steps, unexpected findings, etc. Provide figures showing the results of your simulations, verifying that all of the above specifications have been met. Also, *provide evidence to clearly show that all transistors are operating in saturation*. You will probably want to provide several other figures to help you explain your design methodology. Screen captures are fine (not all figures need to be imported to Matlab – you may not even need to import any data into Matlab if you make full use of the tools available in Cadence).

Quality of Report (5 Points)
Please make sure that all numbers are readable, that the figures are large enough, and that there are no gross errors in terms of grammar, spelling, or punctuation. *A large portion of this project focuses on coming up with a clear design methodology, implementing that design methodology, and then tweaking things as needed. Therefore, please clearly present your design methodology.*

What to Turn In
You only need to turn in an electronic copy for this project. Feel free to turn in a paper copy, but it is not required this time.

Helpful Hints
- Read through this entire project description before starting the project.
- You will be graded on meeting the specifications as well as providing clear methodologies for creating your design.
- Cadence has a fairly steep learning curve, so please do not wait until the last minute to do this project.
- Make sure that no node voltage goes below ground or above V_{dd}.
- Placing your transistor sizes in a table is an easy way to display your designed values.
- There is a PPT on the class website (Projects page) that has basic circuit elements that you can use to create schematics for your report.
- You will probably want to break your design into smaller, easier-to-design components before you put everything together into the full current mirror design.