EE 551 Linear Integrated Circuits
Project 7
Layout
45 Points

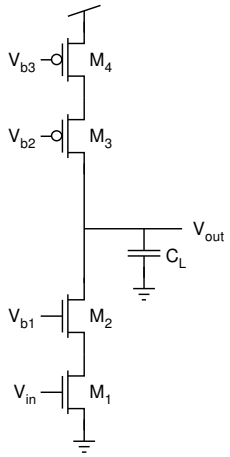
Objective
To learn how to layout analog integrated circuits using industry standard CAD tools.

Work on Your Own
For this project, you are required to work on your own.

CAD Tools
For this project, you will use Cadence to layout and verify your design. Details about how to access and use Cadence are found on the CAD page of the class website.

Part 1 – Cadence Tutorials (0 Points)
In order to layout the amplifier specified in this project, you will need to learn how to use the tools to perform layout. You will be using Cadence for layout and verification. Therefore, you need to go through the remaining tutorials on the class CAD page. It is absolutely critical that you go through all of tutorials 4.1 – 4.4, and you are highly encouraged to go through the rest of the tutorials, since they will be very helpful for the take-home portion of the Final.

Part 2 – Amplifier Layout (40 Points)
Use Cadence to layout the following amplifier with the specified sizes. You are not required to use any matching techniques for this project.



Device Sizes Table (Transistor Sizes in μm)

	M_1 –M_2	M_3 – M_4	C_L
W	4.8	14.4	-
L	1.2	1.2	-
Value	-	-	2pF

You must verify your layout with the standard three verification tools.

- DRC
- Extraction
- LVS

Your design *must* pass DRC and LVS verifications in order for you to get any credit on this part – ie. if your design does not pass these verification steps, it would never be fabricated. You must provide evidence that your design passes DRC and LVS when you hand in your report (screen capture or log files

will suffice). You are not required to do post-layout simulation with your extracted netlist for this project – since I am providing you with the design, you were not even required to perform an initial simulation. However, if this were a real design that you were working on and expecting to send out to fabrication, this would also be a critical step.

The following are two design constraints that apply to your layout.

- You must make your layout as rectangular as possible. In your report, you must provide the dimensions of the smallest rectangle that contains your layout. Maximum points will be given for layout that consumes minimal area (in a *rectangular* shape) while still maintaining good design practices. Good layout practices trump overall chip real estate, however.
- All of your layout pins *must* come out to the edge of the perimeter of the rectangle containing your layout (i.e. your pins must be very obvious and must be easy for the next designer to connect to, if you were passing your cell layout to another engineer who would be using your amplifier). All of these pins should be in the metal1 layer.

Quality of Report (5 Points)

Please make sure that all numbers are readable, that the figures are large enough, and that there are no gross errors in terms of grammar, spelling, or punctuation.

Helpful Hints

- Do not forget substrate and well tie-downs.
- Never underestimate how long layout takes, so do not wait until the last minute.
- You can turn in a log file along with your report, if you would like, to show that LVS worked. Besides that, all else must be contained within your PPT document.