EE 551 Linear Integrated Circuits
Project 8
Layout Matching Techniques
Extra Credit – Up to 35 Points

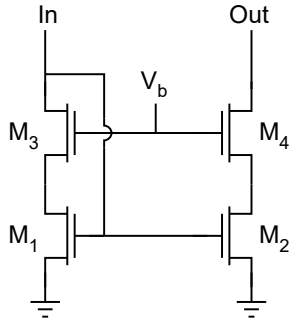
Objective
To learn how to utilize best practices in layout techniques to minimize mismatch effects.

Work on Your Own
For this project, you are required to work on your own.

CAD Tools
For this project, you will use Cadence to layout and verify your design. Details about how to access and use Cadence are found on the CAD page of the class website.

Part 1 – Cadence Tutorials (0 Points)
In order to layout the amplifier specified in this project, you will need to learn how to use the tools to perform layout. You will be using Cadence for layout and verification. Therefore, you need to go through the remaining tutorials on the class CAD page. It is absolutely critical that you go through all of tutorials 4.1 – 4.4, and you are highly encouraged to go through the rest of the tutorials, since they will be very helpful for the take-home portion of the Final.

Part 2 – Current Mirror Using Common-Centroid Layout (Up To 25 Points)
Use Cadence to layout the following current mirror with the specified sizes. You are required to use *common-centroid layout* to minimize mismatch effects. Specifically, M_1 and M_2 must be matched to each other, and M_3 and M_4 must be matched to each other.



Device Sizes Table (Transistor Sizes in μm)

	M_1 and M_3	M_2 and M_4
W	4.8	9.6
L	1.2	1.2

You must verify your layout with the standard three verification tools.

- DRC
- Extraction
- LVS

Your design *must* pass DRC and LVS verifications in order for you to get any credit on this part – ie. if your design does not pass these verification steps, it would never be fabricated. You must provide evidence that your design passes DRC and LVS when you hand in your report (screen capture or log files will suffice). You are not required to do post-layout simulation with your extracted netlist for this project – since I am providing you with the design, you were not even required to perform an initial simulation. However, if this were a real design that you were working on and expecting to send out to fabrication, this would also be a critical step.

You must show several screen shots of your layout to clearly illustrate how you created your current mirror. For example, you may want to include screenshots of your layout at various zoom levels to aid your discussion about your cell that you laid out. You should discuss your design choices for doing your layout. Simply put, I will only be looking at your report (not viewing your cells from within Cadence), so your report should be self-contained – it should show your layout in enough detail that I can clearly see both the details of the individual transistors as well as how they interconnect.

Part 3 – Pad Frame (Up To 10 Points)
Connect your current mirror from Part 2 to the pad frame. Use Pins 1-3 on the pad frame to connect to your current mirror. Please include enough screen shots to clearly show how these connections are made. You will need to watch the tutorial videos on the pad frame and hierarchical schematics / layout in order to do this part of the project.

Helpful Hints

- Do not forget substrate and well tie-downs.
- Never underestimate how long layout takes, so do not wait until the last minute.
- You can turn in a log file along with your report, if you would like, to show that LVS worked. Besides that, all else must be contained within your PPT document.