What You Are Expected To Know

- Basic circuit analysis
  - KVL, KCL, voltage dividers, etc.
  - Basic familiarity with transistors
- Basic signal processing
  - Laplace transforms
  - Frequency response
  - Use of MATLAB
- Basic pn junction device physics
How To Do Well in EE 551

• Come to Class
  – Pay attention
  – Take good notes
  – If I talk about it in class, then it is probably important
  – Do whatever you have to do to stay awake

• Do the homework problems
  – Do them again
  – Do them yet again (These problems are typical of analog IC problems)
  – Hide the solutions when you do them
  – Write out every step
  – Do not assume that if you can follow the solutions you will be able to do the problems at test time

• Start early on the projects
  – Do the individual parts as they are covered in class
  – Do not wait until the last minute

• If you do not understand, then ask questions
  – In class
  – In office hours
Analyze and Design
What Design Really Looks Like
Why Analog?

- Can be much less power than digital
- Can perform many computations faster and more efficiently than digital
- Must be used to interface with outside world
- ~20% of IC market since 1970
“If you’re a 20- to 30-year-old analog engineer, you’re sitting pretty right now. It’s a buyer’s market for you.”

- Freescale Semiconductor
  From IEEE Spectrum, Aug. 2008
Why This Class Is Important To You

Even if you have no plans of going into analog IC design, you will have a hard time not using analog ICs in your work. Understanding the guts of analog IC design will enable you to better evaluate their performance and choose the right parts.
"Analog chips enable computers to interact with the physical world – to see, listen, touch. . .the next ten years will see a shift in emphasis to analog technologies. . .In the coming years, look for analog – not digital – chips to attract the new talent and investment. . ."

- Red Herring Magazine, February 2003
Why Analog for Linear Systems?

The real world is *analog*, so if we need to interface with it, then we *must* have analog circuitry.
Why Integrated Circuits?

- Cheaper (and easier to mass produce)
- Smaller
- Reduces power
- Keeps everything contained
  - Reduces noise
  - Reduces coupling from the environment
- Need a large number of transistors to perform real-world computations/tasks
- Allows a high density of circuit elements (therefore, VLSI reduces costs)
## Difference Between Discrete and IC Design

<table>
<thead>
<tr>
<th></th>
<th>Analog ICs</th>
<th>Discrete Analog</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Device Size and Values</strong></td>
<td>Relatively Small ex. Capacitors 10fF-100pF</td>
<td>Large ex. Capacitors 100pF-100µF</td>
</tr>
<tr>
<td><strong>Resistors</strong></td>
<td>Mostly bad</td>
<td>Easy to Use</td>
</tr>
<tr>
<td></td>
<td>Very expensive (large real estate)</td>
<td>Cheap</td>
</tr>
<tr>
<td><strong>Inductors</strong></td>
<td>Only feasible for very high frequencies</td>
<td>Use when needed</td>
</tr>
<tr>
<td></td>
<td>Extremely expensive</td>
<td></td>
</tr>
<tr>
<td><strong>Parasitics</strong></td>
<td>Very big concern</td>
<td>Exist, but rarely affect performance (Large size of devices and currents)</td>
</tr>
<tr>
<td></td>
<td>Seriously alter system performance</td>
<td></td>
</tr>
<tr>
<td><strong>Matching</strong></td>
<td>Difficult to deal with</td>
<td>Concern</td>
</tr>
<tr>
<td></td>
<td>Major concern</td>
<td>Can more easily match/replace</td>
</tr>
<tr>
<td></td>
<td>Stuck with whatever was fabricated</td>
<td></td>
</tr>
<tr>
<td></td>
<td>ex. 50% mismatch is not uncommon</td>
<td></td>
</tr>
<tr>
<td><strong>Power</strong></td>
<td>Efficient (Small currents pA-mA)</td>
<td>Use more power (Large currents &gt;mA)</td>
</tr>
</tbody>
</table>
Process Considerations

• What processes are...
  – A specific technology for producing integrated circuits
  – Typically specified by their
    • Type (bipolar, CMOS, or BiCMOS)
    • Minimum device size (length) for CMOS (e.g. 0.5µm, 0.35µm)
    • Various other parameters (e.g. maximum/supply voltage, intended disposition – digital or mixed-signal, etc.)
  – Fabricated by a trusted foundry (e.g. AMS, TSMC, etc.)

• Everything is geared towards a digital process
  – Processes not designed with analog in mind
  – Easiest (best method / most flexible) to design with standard process rules
  – Typically not able to construct many analog circuits in a brand new process
Moore’s Law and Its Affect on CMOS Processes

• Moore’s Law (1965)
  – The number of transistors on an integrated circuit doubles every (approximately) 18-24 months

• Processes vs. time
  – Introduction of a new process approximately every two years
    • This shrinks the transistors, so more can fit in a given space
    • Minimum transistor length decreases over time
    • Most digital circuits are purely [minimum-sized] transistors
  – Greatly speeds up processing speeds
  – Greatly reduces power consumption
  – Intended to reduce cost, as well (but new processes can be quite expensive)
Effect of Changing Processes

What changing processes mean (for design)
- Supply voltages drop (big difference)
  - e.g. 0.5µm → $V_{dd} = 3.3\text{V}$; 0.18µm → $V_{dd} = 1.8\text{V}$
  - New techniques for reduced operating range
- Device sizes
  - Transistor sizes decrease with every process
  - Capacitors may not
- Short channel effects
  - Traditional MOSFET models are a poor fit to small devices
- Varying design rules from process to process (submicron processes)
  - Must relearn “design rules” for each process
  - Specific rules to make sure nothing breaks
Bipolar vs. CMOS

Pros for Bipolar
• Work well for analog
• High gain
• High speed

Pros for CMOS
• Cheap, cheap, cheap!
• Scales nicely with Moore’s Law
• Mixed-signal ICs (SOC)
System-On-A-Chip (SOC)

The real reason why CMOS dominates analog ICs – Systems on a chip

Complete Integrated Circuit

- Analog
- Digital

Real designs include both analog and digital portions

- **Digital Portion**
  - Scales nicely with Moore’s Law
  - Straightforward design procedures
  - Uses mostly small transistors (can really pack them in) and very few capacitors

- **Analog Portion**
  - Scaling mostly comes through ingenuity
  - No straightforward/automated design procedures
  - Uses often relatively large transistors and capacitors
  - Consumes a large amount of the chip real estate and design time

Easier, cheaper, and better to do a complete design on a single chip.
To Summarize …

**Good Things about Analog IC Design**
- Inexpensive
- Compact
- Power Efficient

**Not So Good Things about Analog IC Design** *(not necessarily bad)*
- Limited to transistors and capacitors (and sometimes resistors if a very good reason)
- Parasitics and device mismatch are big concerns
- You are stuck with what you built/fabricated (no swapping parts out)
Important Considerations

We will limit our discussion to CMOS technologies
- Only MOSFETs
- Limited use of BJTs

Therefore, we will discuss only silicon processes
• Circuits and systems are *linear* only over a specific range
• We will constantly talk about
  – Large-signal operation
    • Nonlinear equations
    • DC operating point, bias conditions
  – Small-signal analysis
    • Linear equations
    • Amplification region
• Every circuit must be analyzed with *both* the large- and small-signal analyses
**Large-Signal vs. Small-Signal**

Typical Amplifier Transfer Function

- **Gain** = Slope

- **Linear, high-gain region (amplifier)**

- **Nonlinear portions**

- **Must first do a *large-signal analysis* to get the amplifier into range**
  - Bias in the amplification region
  - DC operating point (DC voltages and currents) from the large-signal operation

- **Once in the amplification region, assume a *small-signal* input**
  - Everything will stay within the linear region / linear range
  - Linear, time-invariant (LTI) analysis applies
Large-Signal vs. Small-Signal

- **Large signal (Biases / DC conditions)**
  - Moves amplifier into range
  - Amplifier is now ready to perform amplification
- **Small signal (AC inputs / outputs)**
  - Small sinusoidal inputs makes bigger sinusoidal outputs
Creating Linear Blocks

What are the characteristics of the ideal blocks we need in order to make linear circuits and systems?
## Input / Output Relationships

<table>
<thead>
<tr>
<th>Device</th>
<th>$Z_{in}$</th>
<th>$Z_{out}$</th>
<th>Reason</th>
</tr>
</thead>
<tbody>
<tr>
<td>Independent Voltage Source</td>
<td>-</td>
<td>0Ω</td>
<td>0V output → no voltage drop; no resistance</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0V output → replace with a short circuit</td>
</tr>
<tr>
<td>Independent Current Source</td>
<td>-</td>
<td>$\infty$Ω</td>
<td>0A output → no current flows; infinite resistance</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0A output → replace with an open circuit</td>
</tr>
<tr>
<td>Voltmeter</td>
<td>$\infty$Ω</td>
<td>-</td>
<td>Minimizes loading effects</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>No resistance in parallel</td>
</tr>
<tr>
<td>Ammeter</td>
<td>0Ω</td>
<td>-</td>
<td>Minimizes loading effects</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>No resistance in series</td>
</tr>
<tr>
<td>Voltage-Controlled Voltage Source</td>
<td>$\infty$Ω</td>
<td>0Ω</td>
<td></td>
</tr>
<tr>
<td>Voltage-Controlled Current Source</td>
<td>$\infty$Ω</td>
<td>$\infty$Ω</td>
<td></td>
</tr>
<tr>
<td>Current-Controlled Voltage Source</td>
<td>0Ω</td>
<td>0Ω</td>
<td></td>
</tr>
<tr>
<td>Current-Controlled Current Source</td>
<td>0Ω</td>
<td>$\infty$Ω</td>
<td></td>
</tr>
</tbody>
</table>
Input / Output Impedances

Lessons learned

• Inputs
  – Voltage sensing $\rightarrow$ Want high input impedance
  – Current sensing $\rightarrow$ Want low input impedance

• Outputs
  – Voltage output $\rightarrow$ Want low output impedance
  – Current output $\rightarrow$ Want high output impedance
Input Impedances

- Inputs
  - Voltage sensing → Desire high input impedance
  - Current sensing → Desire low input impedance

**Voltage Sensing**

Norton Equivalent

\[ V_{\text{sense}} = I_N R_N || R_{\text{sense}} \]

\[ V_{\text{sense}} \rightarrow I_N R_N \quad \text{as} \quad R_{\text{sense}} \rightarrow \infty \]

**Current Sensing**

Thevenin Equivalent

\[ I_{\text{sense}} = \frac{V_{Th}}{R_{Th} + R_{\text{sense}}} \]

\[ I_{\text{sense}} \approx \frac{V_{Th}}{R_{Th}} \quad \text{as} \quad R_{\text{sense}} \rightarrow 0 \]

Norton and Thevenin equivalents represent the circuit we are sensing.
Output Impedances

- Outputs
  - Voltage outputs → Desire low output impedance
  - Current outputs → Desire high output impedance

Voltage Output

\[ V_{out} = \frac{V_{Th}}{R_{in} + R_{Th}} \]
\[ V_{out} \approx V_{Th} \quad \text{as} \quad R_{Th} \rightarrow 0 \]

Current Output

\[ I_{out} = I_{N} \frac{R_{N}}{R_{N} + R_{in}} \]
\[ I_{out} \approx I_{N} \quad \text{as} \quad R_{N} \rightarrow \infty \]

Norton and Thevenin equivalents represent the circuit supplying voltage/current. 
\( R_{in} \) represents the input impedance of the subsequent stage.
Ideal Operational Amplifier

Ideal Opamp Model
- Zero input current
  - Infinite input impedance
- Zero output impedance
- $V_{out} = A(V^+ - V^-)$
- Gain is infinite
- If negative feedback, $V^+ = V^-$

Example – Voltage Buffer
- Infinite input impedance
  - No loading on previous circuit
- Zero output impedance
  - No loading on following circuit
- Closed-loop gain = 1
  - Looks like a VCVS
- Completely “buffers” a voltage
  - Passes $V$ from one circuit to another with no loading effects
Two-Port Models

• Most important parameter in an amplifier is **gain**
• Must determine how loading affects gain
• Two-port models simplifies this process

![Two-Port Equivalent](image)

• One parameter at each port is independent
• The other port is dependent on both the first port and the two-port network

Admittance Parameter Equations

• Voltage is independent
• Current is dependent
• (Typical of most “voltage-mode” circuits)

\[
\begin{align*}
    i_1 &= y_{11}v_1 + y_{12}v_2 \\
    i_2 &= y_{21}v_1 + y_{22}v_2
\end{align*}
\]
Two-Port Model Admittance Parameters

\[ y_{11} = \left. \frac{i_1}{v_1} \right|_{v_2=0} \]

Input admittance
Output short circuited

\[ y_{12} = \left. \frac{i_1}{v_2} \right|_{v_1=0} \]

Reverse transconductance
Input short circuited

\[ y_{21} = \left. \frac{i_2}{v_1} \right|_{v_2=0} \]

Forward transconductance
Output short circuited

\[ y_{22} = \left. \frac{i_2}{v_2} \right|_{v_1=0} \]

Output admittance
Input short circuited

\[ i_1 = y_{11}v_1 + y_{12}v_2 \]

\[ i_2 = y_{21}v_1 + y_{22}v_2 \]
Unilateral Two-Port Model

- Typically, there is no feedback $y_{12} = 0$
- $y_{21}$ is referred to as “transconductance” ($G_m$)
- Convert admittances into impedances
  - $Z_{in} = \text{input impedance}$
  - $Z_{out} = \text{output impedance}$

\[
a_v = \left. \frac{v_2}{v_1} \right|_{i_2=0} = -G_m Z_{out}
\]
Connecting a Two-Port Network to a Circuit

Thevenin Source

Two-Port Model

Thevenin Load

\[ a_v = \frac{v_{out}}{v_{in}} = \frac{v_1}{v_{in}} \cdot \frac{v_{out}}{v_1} \]

\[ = \left( \frac{v_{in}}{v_{in} \left( R_{in} + R_s \right)} \right) \left( - \frac{G_m v_1}{v_1} R_{out} \left\| R_L \right\| \right) \]

\[ = \left( \frac{R_{in}}{R_{in} + R_s} \right) \left( - G_m \left( R_{out} \left\| R_L \right\| \right) \right) \]

Assuming \( R_s \) and \( R_L \) are fixed

- \( a_v \uparrow \) as \( R_{in} \uparrow \)
- \( a_v \uparrow \) as \( R_{out} \uparrow \)

Therefore, need high output impedance for high gain

\[ a_v = -G_m Z_{out} \]

But want low output impedance for opamps to reduce loading
Typical Opamp Design

- **Input**: $V_{\text{in}+}$, $V_{\text{in}-}$

- **Stages**:
  - Differential Gain Stage
  - High-Gain Stage
  - Output Stage

- **Output**: $V_{\text{out}}$

- **Output Characteristics**:
  - Low $Z_{\text{out}}$
  - Drives large current
  - Only needed for resistive loads
  - If not included, called an operational transconductance amplifier (OTA)
Complete Opamp Design

One size does not fit all.
The Approach for the Semester…

• Gain appreciation of devices from physics
• Build models of basic devices
• Create small circuits
• Use small circuits to build large circuits
• Focus on opamp design and supporting circuitry