# Simple Opamps

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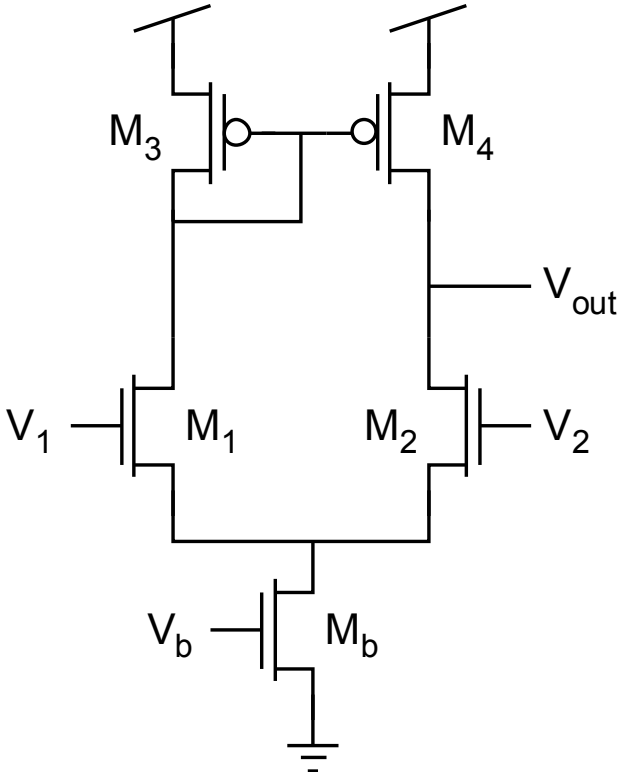
# 5 Transistor Opamp




How are $V_1$ and $V_2$ mapped to $V^+$ and $V^-$?

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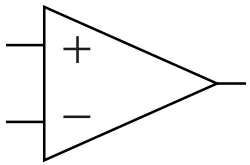
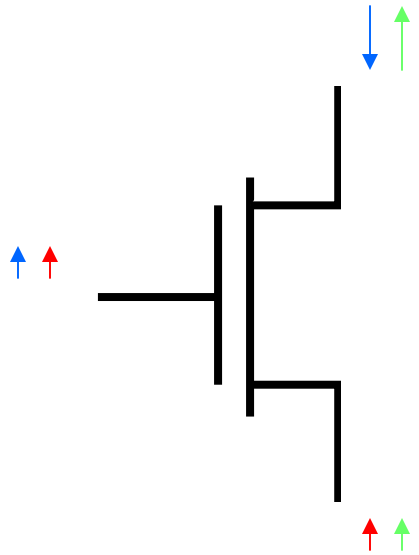
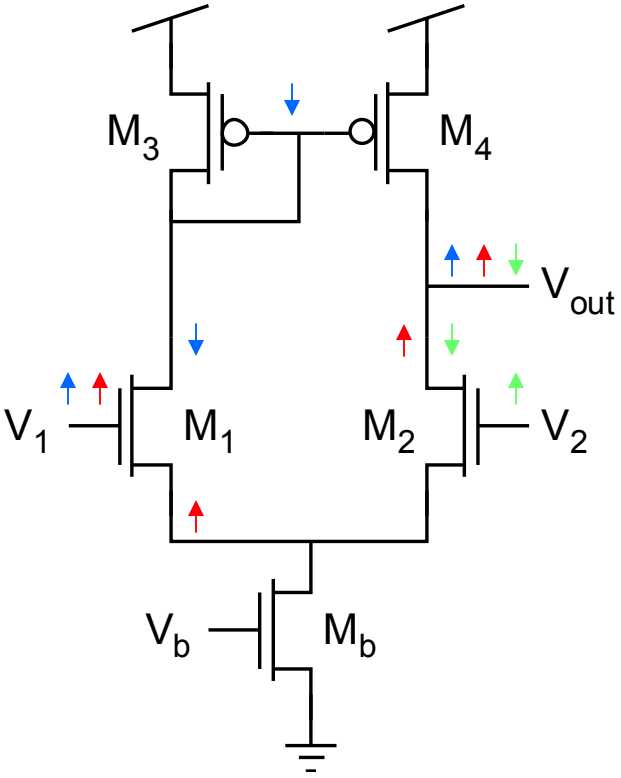


# Signal Tracing

- Determination of +/- terminals
- Need to determine the direction and polarity of signal flow
- Remember the basic amplifiers
  - Nothing ever comes out at the gate
  - CS Amp
    - inverting, large gain
    - input = gate, output = drain
  - CD Amp
    - non-inverting, ~unity gain (slightly condensing)
    - input = gate, output = source
  - CG Amp
    - non-inverting, large gain
    - input = source, output = drain
  - Signal does not flow from drain to source (dead end)



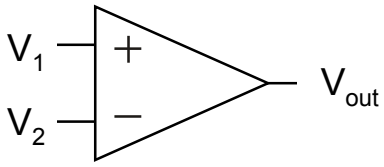
# Signal Tracing Example




If $V_1\uparrow$ then $V_{out}\uparrow \rightarrow V_1$ is the non-inverting input

Double check

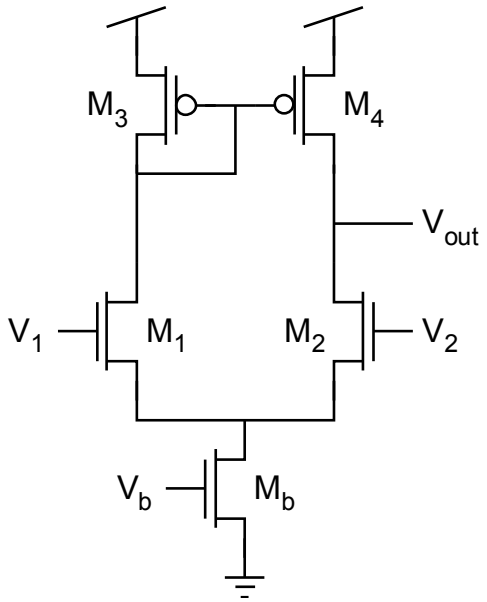
Triple check



# Design

Design Constraints

- Power Supply
- Process
- Temperature




Design Specifications

- Small-signal gain, $A_v$
- Frequency response for a given load capacitance, $\omega_{-3dB}$
- Input common-mode range (ICMR) – $[V_{icm,min}\ V_{icm,max}]$
- Slew rate for a given load capacitance, SR
- Power dissipation, $P_{diss}$

# Design Procedure Relationships

$$A_v = g_{m1} R_{out} = g_{m1} r_{o2} \parallel r_{04}$$

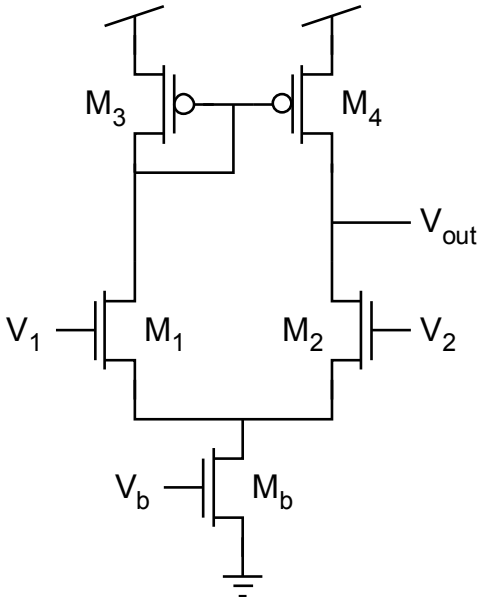
$$\omega_{-3dB} = \frac{1}{R_{out} C_L} = \frac{1}{r_{o2} \parallel r_{04} C_L}$$

$$V_{icm,\max} = V_{dd} - V_{gs3} - V_{ds1,sat} + V_{gs1}$$
$$= V_{dd} - V_{gs3} + V_{T1} \quad \text{(above } V_T\text{)}$$

$$V_{icm,\min} = V_{ds,b,sat} + V_{gs1} = V_{ds,b,sat} + V_{gs2}$$

$$SR = \frac{I_b}{C_L}$$

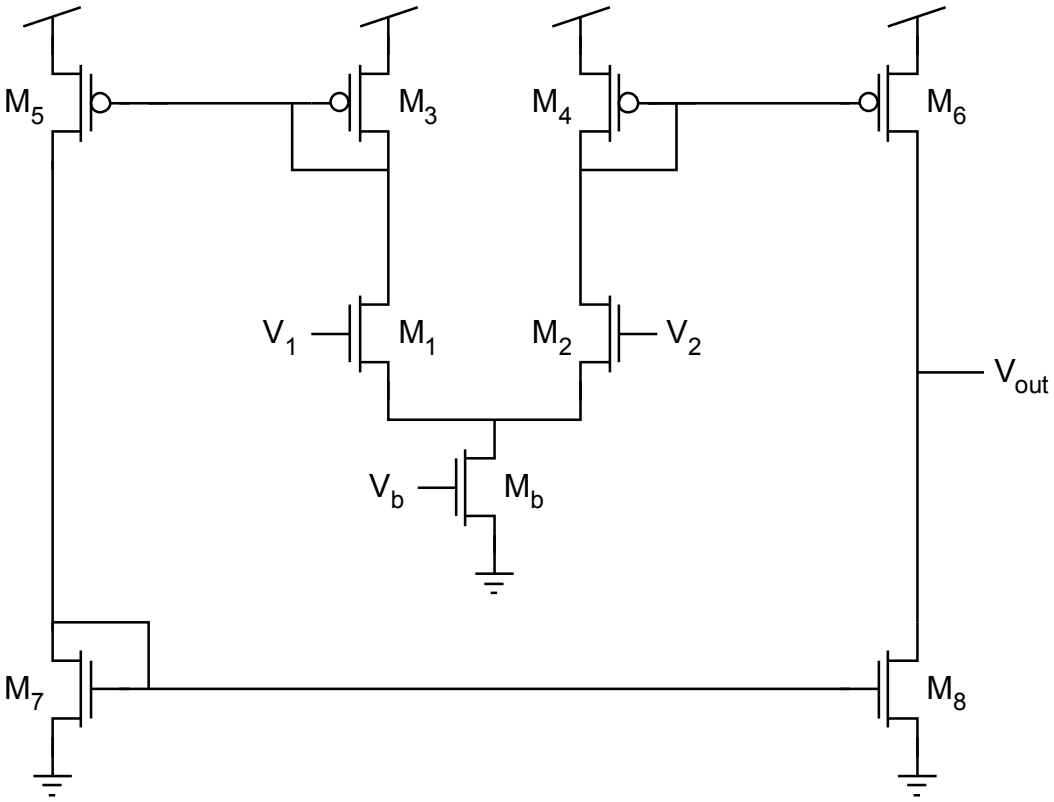
$$P_{diss} = I_b V_{dd} = (I_3 + I_4) V_{dd}$$



# Design Procedure

1. Choose $I_b$ to satisfy the slew rate for a given $C_L$ or the to satisfy the power dissipation, $P_{diss}$
2. Choose $L_2$ and $L_4$ for $R_{out}$ to satisfy $\omega_{-3dB}$ (if feasible…if not, choose a different topology)
3. Design $W_3/L_3$ ($W_4/L_4$) to satisfy the upper limit for ICMR
4. Design $W_1/L_1$ ($W_2/L_2$) to satisfy the small-signal gain, $A_v$
5. Design $W_b/L_b$ to satisfy the lower ICMR
6. Iterate where necessary and tweak in simulation

# Wide-Output Range OTA




Voltage Gain $A_v = g_{m1} r_{o6} \| r_{08}$

ICMR

$$V_{icm,\max} = V_{dd} - V_{gs3} - V_{ds1,sat} + V_{gs1}$$
$$= V_{dd} - V_{gs3} + V_{T1} \quad \text{(above } V_T\text{)}$$

$$V_{icm,\min} = V_{ds,b,sat} + V_{gs1} = V_{ds,b,sat} + V_{gs2}$$

$V_{out}$ Range $\left[V_{ds8,sat} \text{ to } \left(V_{dd} - V_{ds6,sat}\right)\right]$

$V_+$ and $V_-$ Terminals