Overview of Silicon p-n Junctions

Dr. David W. Graham

West Virginia University
Lane Department of Computer Science and Electrical Engineering
© 2009 David W. Graham
p-n Junctions (Diodes)

- Fundamental semiconductor device
- In every type of transistor
- Useful circuit elements (one-way valve)
- Light emitting diodes (LEDs)
- Light sensors ( imagers)
p-n Junctions (Diodes)

Bring p-type and n-type material into contact
p-n Junctions (Diodes)

- All the $h^+$ from the p-type side and $e^-$ from the n-type side undergo diffusion → Move towards the opposite side (less concentration)
- When the carriers get to the other side, they become minority carriers
- Recombination → The minority carriers are quickly annihilated by the large number of majority carriers
- All the carriers on both sides of the junction are depleted from the material leaving
  - Only charged, stationary particles (within a given region)
  - A net electric field
  - This area is known as the depletion region (depleted of carriers)
  - Size of the depletion region depends on the diffusion length
The remaining stationary charged particles result in areas with a net charge.
Electric Field

- Areas with opposing charge densities creates an E-field
- Total areas of charge are equal (but opposite)
- E-field is the integral of the charge density
- Poisson’s Equation

\[
\frac{dE}{dx} = \frac{\rho(x)}{\varepsilon} = \frac{\rho(x)}{K_S \varepsilon_0}
\]

\(\varepsilon\) is the permittivity of Silicon

\[
E = -\frac{dV}{dx}
\]

\[
E_{\text{max}} = -\frac{qN_A}{\varepsilon} x_p = -\frac{qN_D}{\varepsilon} x_n = -\frac{2(V_{bi} - V_A)}{w}
\]
Potential

- E-field sets up a potential difference
- Potential is the negative of the integral of the E-field

\[
\frac{d\psi}{dx} = -E(x)
\]

Built-In Potential
- Integrate the E-field within the depletion region
- Use the Einstein Relation

\[
V_{bi} = \frac{kT}{q} \ln\left(\frac{N_A N_D}{n_i^2}\right)
\]

Let \( U_T = \frac{kT}{q} = 25.9mV \)

\( V_{bi} \) typically in the range of 0.6-0.7V
• Line up the Fermi levels
• Draw a smooth curve to connect them
Asymmetric Doping ($N_A = 4N_D$)
p-n Junction Band Diagram

$V_A$ is the applied bias

$E_C$

$E_F$

$E_V$

p-type

n-type

Depletion Region
p-n Junction – No Applied Bias

If $V_A = 0$

- Any $e^-$ or $h^+$ that wanders into the depletion region will be swept to the other side via the E-field.
- Some $e^-$ and $h^+$ have sufficient energy to diffuse across the depletion region.

If no applied voltage

$$I_{drift} = I_{diff}$$
p-n Junction – Reverse Biased

If $V_A < 0$

- Barrier is increased
- No diffusion current occurs (not sufficient energy to cross the barrier)
- Drift may still occur
- Any generation that occurs inside the depletion region adds to the drift current
- All current is drift current
If $V_A > 0$

- Barrier is reduced, so more e⁻ and h⁺ may diffuse across.
- Increasing $V_A$ increases the e⁻ and h⁺ that have sufficient energy to cross the boundary in an exponential relationship (Boltzmann Distributions).
- Exponential increase in diffusion current.
- Drift current remains the same.

Depletion Region Shrinks
**p-n Junction Diode**

\[ I = I_0 \left( e^{V_A/nU_T} - 1 \right) \]

- Combination of drift and generation
- Diffusion
- Drift

\[ I_0 = qA \left( \frac{D_n}{L_n} \frac{n_i^2}{N_A} + \frac{D_p}{L_p} \frac{n_i^2}{N_D} \right) \]

\[ U_T = \frac{kT}{q} \rightarrow \text{Thermal voltage} = 25.86\text{mV} \]

\[ q = 1.602 \times 10^{-19} \text{C} \]

\[ A = \text{cross-sectional area} \]
\[ I = I_0 \left( e^{V_A / nU_T} - 1 \right) \approx \begin{cases} I_0 e^{V_A / nU_T} & \text{for } V_A > 0 \\ -I_0 & \text{for } V_A < 0 \end{cases} \]

\[ \frac{I}{I_0} = e^{V_A / nU_T} - 1 \]

\[ \frac{1}{nU_T} = \frac{q}{nkT} \]

\[ \ln \left( \frac{I}{I_0} \right) = \ln \left( e^{V_A / nU_T} \right) \]

\[ \ln(I) = \ln \left( e^{V_A / nU_T} \right) + \ln(I_0) \]

\[ \ln(I) = \frac{V_A}{nU_T} + \ln(I_0) \]
Curve Fitting Exponential Data (In MATLAB)

\[ I \approx I_0 e^{V_A/nU_T} \]

- Given I and V (vectors of data)
- Use the MATLAB functions
  - `polyfit` – function to fit a polynomial (find the coefficients)
  - `polyval` – function to plot a polynomial with given coefficients and x values

\[
\begin{align*}
[A] &= \text{polyfit}(V, \log(I), 1); \\
\text{polyfit(independent\_var, dependent\_var, polynomial\_order)} \\
\text{A(1) = slope} \\
\text{A(2) = intercept}
\end{align*}
\]

\[
[I\_fit] = \text{polyval}(A, V); \\
\text{draws the curve-fit line}
\]
Size of the Depletion Region

\[ x_n = \left[ \frac{2K_s \varepsilon_0}{q} \frac{N_A}{N_D(N_A + N_D)}(V_{bi} - V_A) \right]^{\frac{1}{2}} \]

\[ x_p = \left[ \frac{2K_s \varepsilon_0}{q} \frac{N_D}{N_A(N_A + N_D)}(V_{bi} - V_A) \right]^{\frac{1}{2}} \]

\[ w = x_n + x_p = \frac{N_D}{N_A} x_n \]

Depends on
• Doping
• Applied voltage

Depletion region extends farther into the more lightly doped side.

\[ V_A = \text{Applied voltage} \]
\[ V_A = 0 \text{ under equilibrium conditions} \]

\[ q = \text{Unit of charge} \]
\[ q = 1.602 \times 10^{-19} C \]

\[ K_s = \text{Semiconductor dielectric constant} \]
\[ K_s = \text{Relative permittivity} \]
\[ K_s = 11.8 \text{ (Silicon)} \]

\[ \varepsilon_0 = \text{Permittivity of free space} \]
\[ \varepsilon_0 = 8.854 \times 10^{-12} F/m \]

\[ w = \text{Width of depletion region} \]
Size of the Depletion Region

Asymmetric Doping
- One side of the p-n junction is more heavily doped
- Depletion region extends mostly into lightly doped side
- Common in CMOS processes
- Ex. $N_A >> N_D$

$$x_n = \left[ \frac{2K_s \varepsilon_0}{qN_D} (V_{bi} - V_A) \right]^{1/2}$$

$$\frac{x_n}{x_p} \approx \frac{N_A}{N_D}$$
Reverse-Biased p-n Junction Capacitance

- With reverse-biased diodes, there is very small current flow (neglect)
- (Forward-biased diodes must account for movement of charge)
- Total charge in depletion region given by width of depletion region times concentration of immobile charge
- Capacitance definition

\[ C = \frac{\varepsilon A}{d} \]

- Junction Capacitance

\[ C_J = \frac{K_s \varepsilon_0 A}{W} \]

\( A \rightarrow \) cross-sectional area (i.e. the semiconductor has depth (3-D))
Small-Signal Reverse-Biased Capacitance

Small changes in $V_A$ around a DC bias value
- Small change in charge ($Q$) around a baseline level of charge (on each side of the junction)
- Results in a “small-signal” capacitance, $C_j$
- Baseline charge in the depletion region

$$Q^+ = \left[2qK_s\varepsilon_0 \frac{N_A N_D}{N_A + N_D} (V_{bi} - V_A) \right]^{1/2}$$
on the n-type side

$$Q^- = Q^+$$ (charge must be offset)
Small-Signal Reverse-Biased Capacitance

Small changed in charge (for $V_A = 0$) is the small-signal capacitance

$$C_j = \frac{dQ^+}{dV_A} = \left[ \frac{qK_s \epsilon_0}{2(V_{bi} - V_A)} \frac{N_A N_D}{N_A + N_D} \right]^{1/2} = \frac{C_{j0}}{\sqrt{1 + \frac{V_A}{V_{bi}}}}$$

Zero-bias junction capacitance

$$C_{j0} = \sqrt{\frac{qK_s \epsilon_0 N_A N_D}{2V_{bi} (N_A + N_D)}}$$

$C_{j0}$ $\rightarrow$ Depletion capacitance per unit area at $V_A=0$

$V_A$ is the reverse bias here (i.e. $V_A>0$ for a reverse bias)
Small-Signal Reverse-Biased Capacitance

One-Sided Junctions

- Lightly doped on one side
- Common case with substrate/well

\[ C_j = \frac{dQ^+}{dV_A} = \sqrt{\frac{qK_s\varepsilon_0N_D}{2(V_{bi} - V_A)}} = \frac{C_{j0}}{\sqrt{1 + \frac{V_A}{V_{bi}}}} \quad \text{for } N_A >> N_D \quad V_A < 0 \]

\[ C_{j0} = \sqrt{\frac{qK_s\varepsilon_0N_D}{2V_{bi}}} \]

Smaller depletion capacitances for more lightly doped substrates
Therefore, immobile charge on each side of a reverse biased substrate

\[ Q = 2C_{j0}V_{bi}\sqrt{1 + \frac{V_A}{V_{bi}}} \quad \text{for } V_A < 0 \]
Small-Signal Reverse-Biased Capacitance

- $C_j$ is a nonlinear capacitance
- Decreases with increasing reverse bias

![Graph showing the relationship between $C_j$ and $V_A$.]
Large-Signal Reverse-Biased Junction Capacitance

- Approximate with an average value
- Use two extreme values for the average

\[
C = \frac{Q}{V} = \frac{Q(V_2) - Q(V_1)}{V_2 - V_1} \quad \text{(Average)}
\]

\[
\therefore \quad C_{j-av} = \frac{2C_j V_{bi}}{V_2 - V_1} \left( \sqrt{1 + \frac{V_2}{V_{bi}}} - \sqrt{1 + \frac{V_1}{V_{bi}}} \right)
\]

Rough ballpark estimate

\[
C_{j-av} = \frac{C_j}{2}
\]
Forward-Biased Junction Capacitance

- Appreciable amount of current flowing
- More carriers present at the edges of the depletion region
- Therefore, total capacitance is composed of
  - \( C_j \rightarrow \) Junction Capacitance
  - \( C_d \rightarrow \) Depletion Capacitance

\[
C_T = C_j + C_d
\]

where

\[
C_j \approx 2C_{j0}
\]

\[
C_d \gg C_j \quad \text{(typically)}
\]

\[
C_d = \tau_t \frac{I_D}{U_T}
\]

\( \tau_t \rightarrow \) Transit time of diode
\( \tau_t \rightarrow \) Given parameter for a specific process

\[
\tau_t = \frac{L_x^2}{D_x}
\]

where \( x \) is the more heavily doped side.
Small-Signal Junction Resistance

Change in diode voltage as the forward-bias current changes

\[
\frac{1}{r_d} = \frac{dI_D}{dV_D} = \frac{d}{dV_D} \left( I_0 e^{V_D/nU_T} \right) = \frac{1}{nU_T} I_0 e^{V_D/nU_T} = \frac{I_D}{nU_T}
\]

\[\therefore r_d = \frac{nU_T}{I_D} \]
Small-Signal Equivalent Model

- For small changes around a DC bias
- For forward-biased p-n junctions

\[ r_d = \frac{nU_T}{I_D} \quad C_T = C_j + C_d \quad C_j \approx 2C_{j0} \quad C_d = \tau_t \frac{I_D}{U_T} \quad \tau_t = \frac{L_x^2}{D_x} \]
Bipolar Junction Transistors (BJTs)

- Two back-to-back p-n junctions
- Either npn or pnp
- Not the focus of this class
  - However, they are inherent in CMOS processes (parasitically)
  - Can be useful in reference circuits
  - Can cause problems (latchup)

<table>
<thead>
<tr>
<th>Emitter</th>
<th>Base</th>
<th>Collector</th>
</tr>
</thead>
<tbody>
<tr>
<td>n</td>
<td>p</td>
<td>n</td>
</tr>
</tbody>
</table>

- Typically biased in “forward active” mode
  - BE junction forward biased
  - BC junction reverse biased
BJT Band Diagram

- Virtually no current from C to B
- Exponential change in current from E to B based upon $V_{BE}$ (just like forward biased diodes)
- Current flows from E to C
- B modulates how much current flows
BJT Equations

BJT Equations (Forward Active)

\[
\begin{align*}
I_C &= I_s e^{V_{BE}/U_T} = \alpha_F I_E \\
I_E &= \frac{I_S}{\alpha_F} e^{V_{BE}/U_T} = (\beta + 1) I_B \\
I_C &= \beta I_B \\
\beta &= \frac{\alpha_F}{1 - \alpha_F}, \quad \alpha_F = \frac{\beta}{\beta + 1}
\end{align*}
\]

Typical Values

\[
\begin{align*}
\beta &= 100 \\
\alpha_F &= 0.99
\end{align*}
\]

Almost all current is passed from E to C.

Very little B current

\(I_s, \alpha, \beta\) are constants
Designable BJT Parameters

Designable Parameters
- Emitter Area, $A_E$
- Base Width, $W$
- (These may not be designable in CMOS processes)

For npn transistor

$$I_s = \frac{A_E q D_n n_i^2}{W N_A}$$

$$\beta = \frac{D_n N_D L_p}{D_p N_A W}$$

If pnp, swap the following subscripts
- $n \leftrightarrow p$
- $D \leftrightarrow A$