EE 551 Linear Integrated Circuits Name Solutions
Test 2 April 8, 2014

RULES

This is a closed book, closed notes test. You are, however, allowed one new piece of paper (front and back) of handwritten notes and definitions, but no sample problems, plus your equations sheet from Test 1. You must staple your equations sheets to the back of your test when you hand your test in.

You are permitted to use a calculator.

You have 75 minutes to complete the test. Please read through the entire test before starting, and read through the directions carefully. To receive partial credit, you must show your work.

There is to be absolutely no cheating. Cheating will not be tolerated.

If you have any questions, please raise your hand, and I will come to you to answer them. Do not hesitate to ask questions.

Useful Parameters (Use Unless Otherwise Specified)			
$n_i=10^{10}cm^{-3}$	$\mu_n=1360cm^2/Vs$	$\mu_p=460cm^2/Vs$	$\tau_n=\tau_p=100\mu s$
$K_s=11.8$	$\varepsilon_0=8.854x10^{-12}F/m$	T=300K	$E_g=1.12eV$
$\lvert V_{T0}\rvert = 0.7V$	$\gamma = 0.45V^{1/2}$	$2\varphi_F = 0.9V$	$I_{th} = 1\mu A$
$\kappa_n = \kappa_p = 0.65$ (subV$_T$)	$\kappa_n = \kappa_p = 1$ (above V$_T$)	$I_0 = 1pA$	$K = 100\mu A/V^2$
$V_A = 50V$	$V_{dd} = 5V$	$q = 1.602x10^{-19}C$	m = 1 (for C_{sb0}, C_{db0})
$C_{sb0} = C_{db0} = 10fF$	C_{sb0},C_{db0} incl C_{j0},C_{jsw0}	$C_{ox} = 3.5fF/\mu m^2$	$C_{ov} = 0.1fF/\mu m$
C_{sb0},C_{db0} include area	$V_{bi} = 0.7V$		
1m = 100cm	$1m = 1x10^3mm$	$1m = 1x10^6\mu m$	$1m = 1x10^9nm$
$1x10^{12}pm$	$1x10^{15}fm$	$1x10^{18}am$	

Problem	Value	Score
1	30	
2	10	
3	10	
4	20	
5	25	
6	10	
Total	100/105	

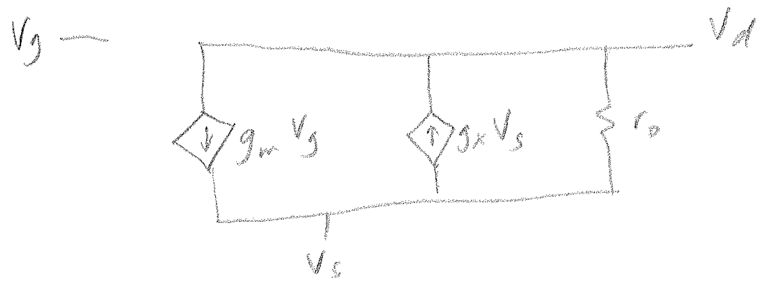
EE 551 Linear Integrated Circuits
Test 2

Name Solutions
April 8, 2014

PROBLEM 1 (30 Points)

An nFET (W=10μm, L=2μm) is biased in saturation such that 10nA flows through it.

A. Draw the low-frequency small-signal model for this transistor. (4 Points)



B. Calculate the transconductance of this transistor under this bias. (2 Points)

$1nA < I_{th}$
∴ subthreshold

$$g_m = \frac{\kappa I}{U_T} = \frac{(0.65)(10nA)}{0.0259V} = 251\ nS$$

C. Calculate either g_s or g_{mb} for this transistor under this bias, whichever is more appropriate. (2 Points)

g_s → subthreshold

$$g_s = \frac{I}{U_T} = \frac{10\ nA}{0.0259V} \approx 386\ nS$$

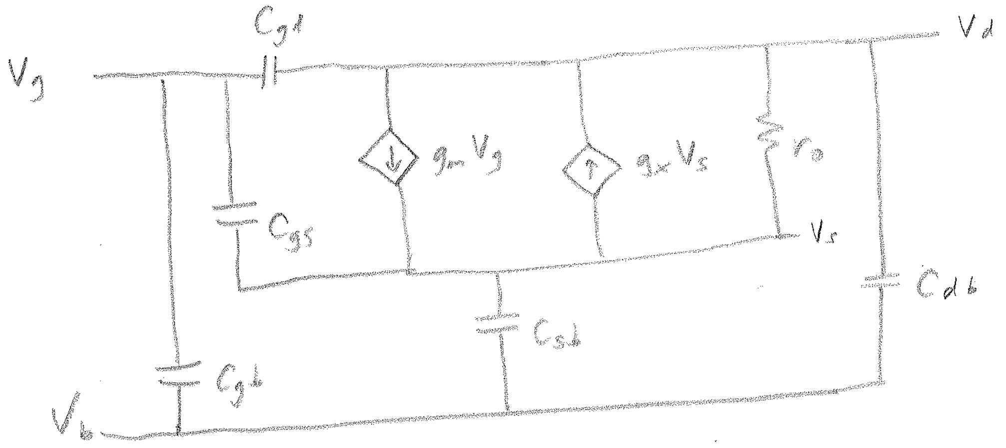
D. Calculate the output resistance of this transistor under this bias. (2 Points)

$$r_o = \frac{V_A}{I} = \frac{50V}{10nA} = 5\ G\Omega$$

E. Calculate the maximum intrinsic gain of this transistor under this bias. (2 Points)

$$-g_m r_o = -1255$$

F. Draw the complete high-frequency small-signal model for this transistor. (5 Points)



G. Calculate the value of all parasitic capacitances for this transistor that can be calculated with the information that has been provided. If any parasitic capacitances cannot be calculated, explain what information is needed to enable calculation of those capacitances to be carried out. (10 Points)

C_{db} and C_{sb} cannot be calculated because the values of V_s and V_d are not known

$C_{gs} = C_{gd} = C_{ov} \cdot W$ (sub V_T)

$= (0.1 fF/\mu m)(10 \mu m) = \boxed{1 fF}$

$C_{gb} = WL(1-\chi)C_{ox} = (10 \mu m)(2 \mu m)(1-0.65)\, 3.5 fF/\mu m^2 = \boxed{24.5 fF}$

H. Can the transition frequency, f_T, be calculated? If so, calculate f_T. If not, why can it not be calculated? (3 Points)

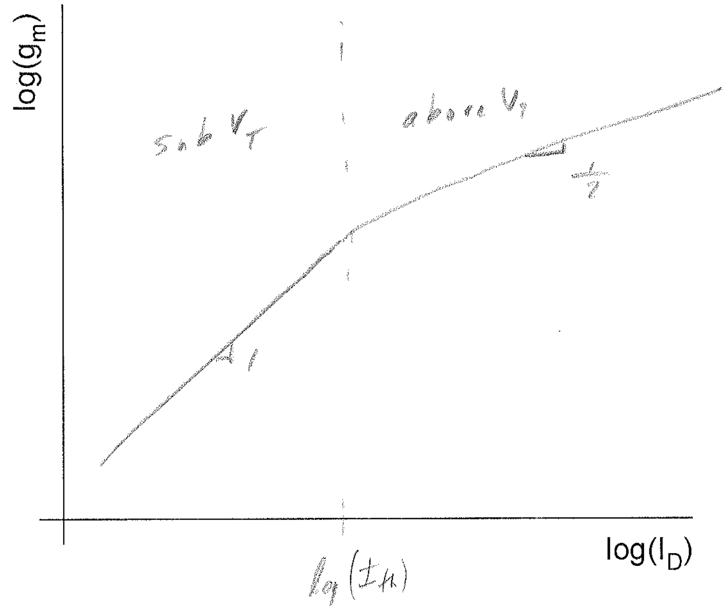
Yes → g_m & the three parasitic capacitances connected to the gate are known

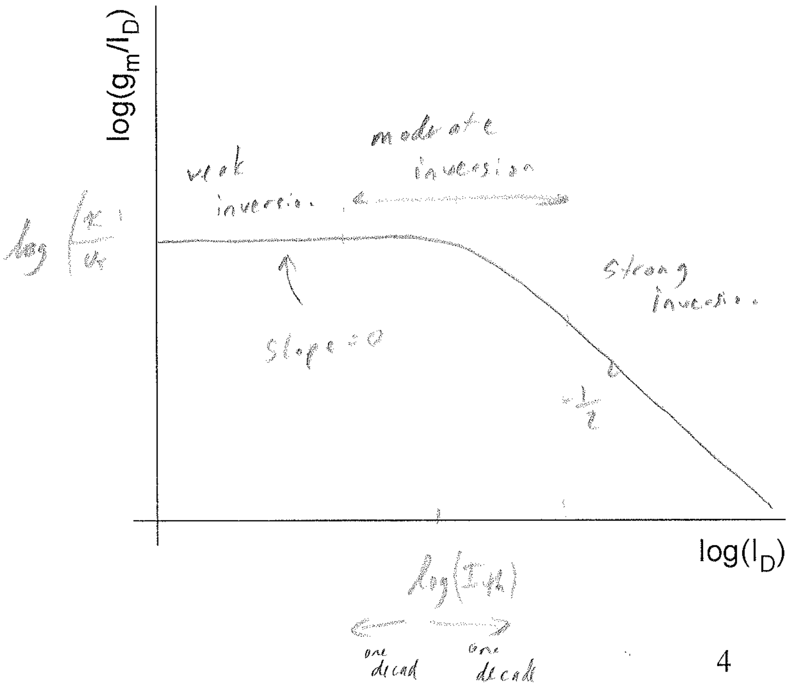
$$f_T = \frac{g_m}{(2\pi)(C_{gs} + C_{gd} + C_{gb})}$$

$$= \frac{251 nS}{(2\pi)(1 fF + 1 fF + 24.5 fF)} = 1.507 MHz$$

PROBLEM 2 (10 Points)

For an nFET transistor, plot the transconductance vs. bias current and the transconductance efficiency vs. bias current on the axes below. Be sure to label all slopes, transition points, regions of operation (e.g., subtheshold), etc. In short, label everything with regard to these two plots.





PROBLEM 3 (10 Points)

Compare and contrast the BSIM and EKV simulation models. Include a discussion of how each of these two simulation models mathematically model a transistor (e.g., how much is the model based upon physics, etc.). Be sure to include a discussion of the strengths and weaknesses of these two simulation models. *Be thorough.*

See discussion from class.

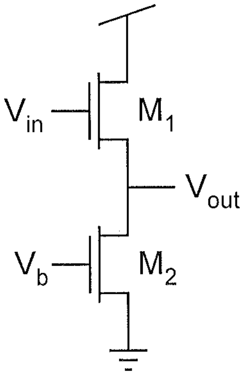
EE 551 Linear Integrated Circuits
Test 2

Name Solutions
April 8, 2014

PROBLEM 4

(20 Points)

Answer the following questions regarding the simple amplifier shown below. Assume that V_b is a fixed (i.e., DC) bias potential.



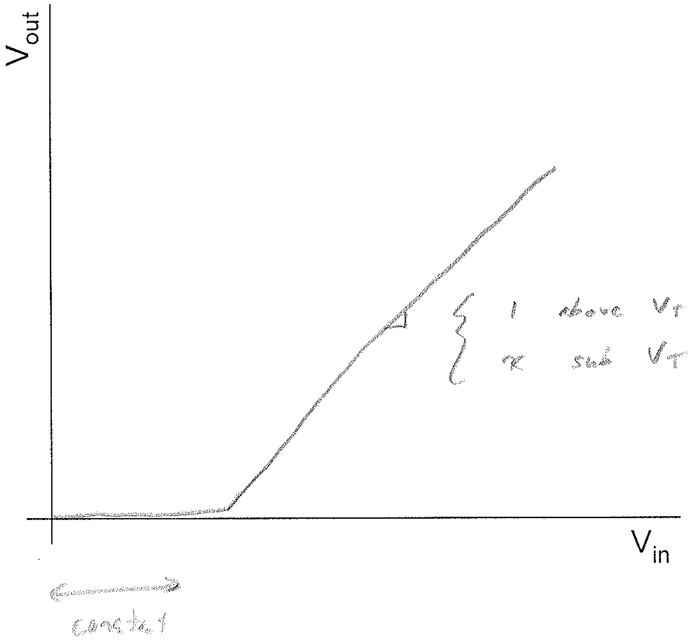
A. What is a name for the basic amplifier stage shown here? (2 Points)

Source Follower
or
Common-Drain Amplifier

B. This amplifier has high / infinite (high/medium/low) input impedance. (1 Point)

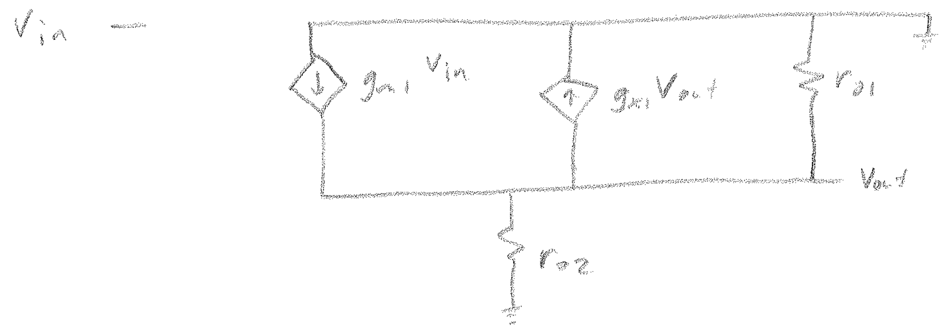
C. This amplifier has low (high/medium/low) output impedance. (1 Point)

D. Sketch the general shape of the voltage transfer function (V_{out} vs. V_{in}). (3 Points)

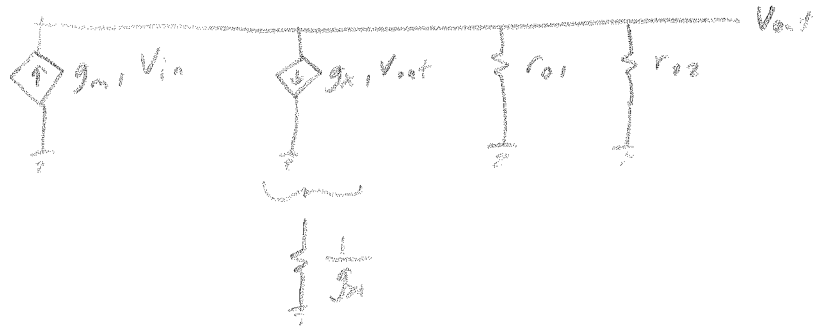


E. Draw the complete small signal model of this amplifier. Indicate if you are using a bulk-referred or source-referred model. (5 Points)

Bulk-Referred Model



F. If V$_b$ is set such that 10nA is flowing through transistor M$_2$, calculate the exact value of the gain. (Calculate means to provide a numerical answer.) (8 Points)



$10nA < I_{th}$
$\Rightarrow$ sub V_T

$$\frac{V_{out}}{V_{in}} = g_{m1}\left(\frac{1}{g_{x1}} \parallel r_{o1} \parallel r_{o2}\right) \approx \frac{g_{m1}}{g_{x1}} = \frac{\frac{\kappa I}{U_T}}{\frac{I}{U_T}} = \kappa = 0.65$$

EE 551 Linear Integrated Circuits
Test 2

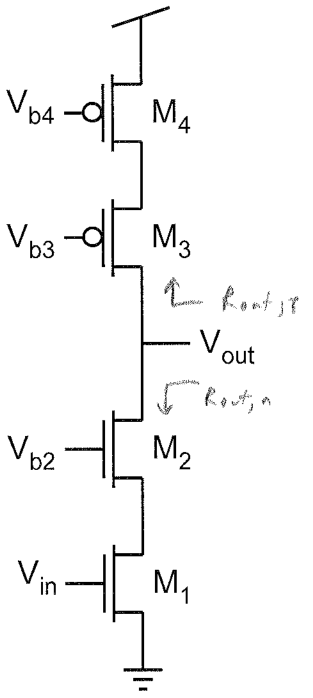
Name Solutions
April 8, 2014

PROBLEM 2 (25 Points)

Using the amplifier shown below, calculate values for the input resistance, output resistance, and voltage gain. Assume that V_{b2}, V_{b3}, and V_{b4} are fixed (i.e., DC) bias potentials and all transistors operate in saturation. Additionally, assume that M_4 is biased such that 100nA flows through it. (Hint – since you are calculating numerical values instead of providing an exact analytic expression, you may make use of appropriate approximations.)

Using these same biasing conditions, calculate the maximum and minimum values that V_{out} can have while still ensuring that all transistors remain in saturation.

$100nA < I_{th} \Rightarrow$ Subthreshold



Numerical Values

R_{in} = $\infty\ \Omega$ ← gate of a MOSFET

R_{out} = 482.63 GΩ

a_v = 1,211,390

$V_{out,max}$ = 4.8 V $V_{dd} - 2\underbrace{V_{ds,sat}}_{100mV}$

$V_{out,min}$ = 200mV ground $+ 2\underbrace{V_{ds,sat}}_{100mV \text{ in subV}_t}$

You could do a rigorous small-signal model, but this is just a cascode configuration in subthreshold.

$$G_m \approx g_{m1} = \frac{\kappa I}{U_T} = \frac{(0.65)(100nA)}{0.0259V} = 2.51\mu S \qquad R_{out} = R_{out,n} \| R_{out,p}$$

$$R_{out,n} = r_{o1} + r_{o2} + g_{x2} r_{o1} r_{o2} \approx g_{x2} r_{o1} r_{o2}$$

$V_{ds,sat} = 100mV$ for all 4 transistors

$$r_{o1} = r_{o2} = r_{o3} = r_{o4} = \frac{V_A}{I} = \frac{50V}{100nA} = 500M\Omega$$

$$g_{x2} = \frac{I}{U_T} = \frac{100nA}{0.0259V} = 3.86\mu S$$

$$R_{out,n} \approx (3.86\mu S)(500M\Omega)(500M\Omega) = 965.25 G\Omega$$

$$R_{out,p} = R_{out,n}$$

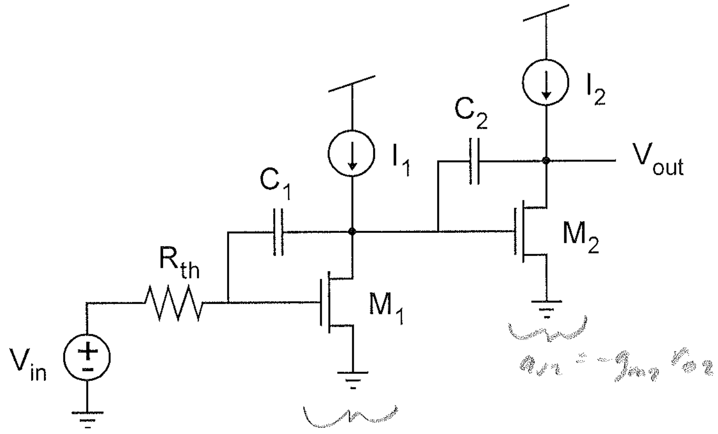
$$R_{out} = R_{out,n} \| R_{out,p} = \tfrac{1}{2} R_{out,n} = 482.63 G\Omega$$

$$a_v = -G_m R_{out} = (2.51\mu S)(482.63 G\Omega) = 1,211,390$$

Problem 5 Work Page

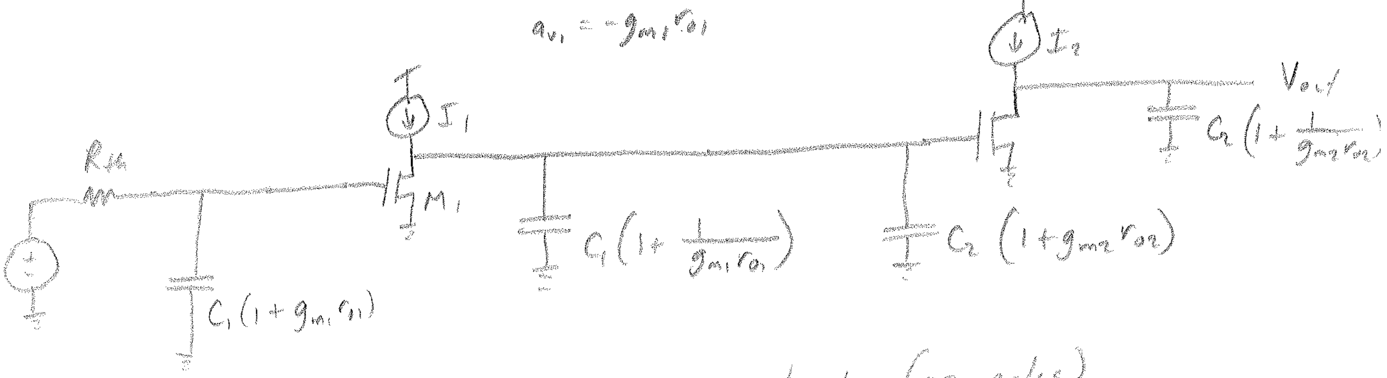
PROBLEM 6 (10 Points)

Use the Miller Theorem to determine all poles in the following circuit. You do not need to include parasitic capacitance. Include only the capacitors that are shown in the figure below.



$$a_{v2} = -g_{m2} r_{o2}$$

$$a_{v1} = -g_{m1} r_{o1}$$



There are 3 nodes, so there are 3 time constants (or poles)
Write as time constants (you could also write as frequencies or poles)

$$\tau_1 = (R_{th})\left(C_1(1+g_{m1} r_{o1})\right)$$

$$\tau_2 = (r_{o1})\left(C_1\left(1+\frac{1}{g_{m1} r_{o1}}\right) + C_2(1+g_{m2} r_{o2})\right) \approx r_{o1}\left(C_1 + C_2(1+g_m r_{o1})\right)$$

$$\tau_3 = (r_{o2})\left(C_2\left(1+\frac{1}{g_{m2} r_{o2}}\right)\right) \approx r_{o2} C_2$$