EE 591L – Neuromorphic Analog VLSI
Project 2 – MOSFETs in the Subthreshold Regime

Objective
To become familiar with subthreshold operation of MOSFETs and also simulation techniques using SPICE.

Simulation Models
This project makes use of simulation using SPICE. In this project, and all subsequent projects requiring simulation, we will be using the EKV model for MOSFETs because it correctly handles both subthreshold and above-threshold currents very well.

You may download the EKV model from the EKV website. We will be using the model developed for a generic 0.5µm process. A direct link to the model is provided on the class website.

For use in your SPICE simulations, you may either copy the entire contents of the model file into your SPICE deck, or you may reference it with a `.INCLUDE` command. The EKV model is level 44 for WinSPICE (which is the default value) and level 55 for HSPICE (you must change this value in two places – one for the nMOS model and one for the pMOS model)

With a 0.5µm process, as we are using for our simulations, the supply voltage (V_{dd}) is 3.3V.

In this project, and all subsequent projects, you must state in your project report which simulator you are using (either WinSPICE or HSPICE).

Suggestion (Nor Required, But Probably Helpful)
In this project (and also later projects), you will be extensively making use of curve fitting tools in MATLAB, just as you did in Project 1. To reduce the amount of work required doing repetitive tasks, it may be helpful to write a simple MATLAB function that is able to curve fit data over a selected range of values using `polyval` and `polyfit`.

Part 1 – Gate Characteristics of a MOSFET
In this part, you will explore the gate characteristics of a MOSFET transistor by sweeping the gate voltage of three different nFETs in SPICE.

For the setup, use a DC sweep to sweep the gate voltage from 0V to V_{dd}. Ground the source, and connect the drain to V_{dd}.

Simulate three differently sized MOSFET transistors such that the W/L ratio meets each of three conditions

- $W/L > 1$
- $W/L = 1$
- $W/L < 1$

You may use transistor sizes (W and L sizes) of any size you desire as long as the sizes fall within the range of 0.6µm - 1000µm. That's a very large range to choose from, but any of these

values could be used in a real design. The low end (0.6μm) represents the minimum length allowable in a 0.5μm process (hence the reason this is sometimes referred to as a 0.6μm process). The upper end is a LARGE transistor (but they can, and sometimes do, go larger than that). Feel free to play around with these values to get a feel for how the width and length and also the ratio of the width to length affect the transistor's operation. For the simulations that you turn in, make sure your choices clearly show the differences in operation, and clearly indicate what values of W and L you have chosen. Additionally, while you have the option to choose any W and L that you like, you *must* keep the size of W constant (you may only change the length of the device to meet the above-given W/L criteria).

Perform gate sweeps for each of these three transistors. (As a general rule, you should always plot the outputs of your simulations with the curve fits overlaying the simulation data.) If you set this up correctly, you can do all three transistors at once.

Additional questions to answer for this part.

- *Approximate* the value of the threshold voltage and the threshold current for each transistor. How do they compare?
- Assuming room-temperature operation, extract the values of kappa and I_0 for each transistor.
- Determine the values of I_0' for each transistor, as well. How do these values compare for each transistor? Why? (Remember, $I_0 = I_0'(W/L)$)
- Turn in a table that summarizes these extracted data values (you should add the pertinent information from Parts 2 and 3 to this table, as well).
- You should have a single plow showing all three transistor sweeps and their resulting curve fits.

Part 2 – Source Characteristics of a MOSFET

Use the same three transistors as you used in Part 1. Perform a source sweep (DC sweep) while biasing the transistor in an above-threshold current (see the curves from Part 1).

- *Approximate* the value of the threshold voltage and the threshold current for each transistor (just approximate this value – curve fitting comes in the next step). How do these values compare to the values you found with the gate sweep? How did you determine these values?
- Extract the values of the thermal voltage for each case. How close was the approximation of room temperature that we used in Part 1? How does this affect your values of kappa?

Part 3 – Drain Characteristics of a MOSFET

Use the same three transistors as you used in Part 1. Perform a drain sweep (DC sweep) while biasing the transistor such that the source is ground. Use three different subthreshold gate voltages for each of the three transistors. You will, therefore, have a family of drain sweeps for each of your three transistors.

- Determine the range of voltages of the drain over which the transistor operates in the ohmic region.
- Determine the saturation current for each case.

- Determine the Early voltage for each case. Do the three Early voltage calculations agree for each transistor.
- Plot the Early voltage versus transistor length. What type of relationship does the Early voltage have to the transistor length and why? You may need to simulate transistors of other lengths to obtain more data points (probably at least five data points are necessary).

Part 4 – nFET Summary Questions

- Typical W/L ratios for most MOSFET transistors are W/L > 1. Can you give a good explanation why this is?
- How do the design parameters (W and L) affect the drain dependence of a MOSFET? With this in mind, how would you design a transistor to act as a reliable current source?

Part 5 – pFET Gate Sweeps

Repeat Part 1, but use pFETs instead using the same three transistor sizes. Extract values for kappa (assuming room temperature), I_0, and I_0'. Also, approximate the threshold voltage (with respect to V_{dd}) and the threshold currents. How do these values differ from nFETs?

Part 6 – Additional pFET Sweeps (Optional – NOT Required)

…but you may find it helpful.

- Perform a source sweep of a pFET
  - How does this curve differ from the nFET case?
- Perform a drain sweep of a pFET with a subthreshold current
  - How does this curve differ from the nFET case?
- Sweep the well potential of the pFET. What does this do?