EE 591L – Neuromorphic Analog VLSI
Project 7 – Physical Layout Design

Objective
To become familiar with integrated circuit layout design.

Special Instructions for This Project
While you are still required to turn in a report for this project, the emphasis of this project should be placed on the actual layout design. The report should be brief and should focus on your approach to the layout.

Part 1 – Cadence Tutorials
A large part of this project will involve simply going through the tutorials on how to use Cadence for integrated-circuit design. These video tutorials are available on the class website along with instructions on how to start and run Cadence.

Part 2 – OTA Layout
Create a schematic for, and then lay out a wide-range OTA (9-transistor OTA) where the transistors have the following dimensions.

- Input transistors: W=48µm, L=1.2µm
- All other transistors: W=4.8µm, L=1.2µm

Ensure that your layout passes DRC and LVS verification checks. These will be checked!

A few specific details about your designs.

- All terminals must be in a metal layer (metal1 or metal2).
- You are not permitted to use metal3 in this project.

You should minimize the area that you are using for your design. Highest points will be awarded to those who have compact designs and follow good layout practices.

Part 3 – Integrate-and-Fire Neuron Layout
Lay out an integrate-and-fire neuron in which the devices have the following dimensions, and create the appropriate schematic, as well.

- C_1 = 1pF
- C_2 = 500fF
- All transistors: W=1.8µm, L=1.2µm

Ensure that your layout passes DRC and LVS verification checks. These will be checked!

A few specific details about your designs.

- All terminals must be in a metal layer (metal1 or metal2).
- You are not permitted to use metal3 in this project.

Extra Credit Opportunity (Up to 20 Extra Points)
For Part 3 (Integrate-and-Fire Neuron), try to make the layout as compact as possible. The group with the most compact layout in terms of overall area will be awarded 10 extra points. The group with the second most compact design will be awarded 5 extra points on this project.

Additionally, both these groups will be invited to show their layout in class and discuss the tradeoffs between "good layout practices" and compactness that they used in their design, and from this very brief presentation, you may earn up to an additional 10 points.

As a result, you must state the x and y dimensions of your layout in your project report, as well as give the total area for this cell.

What to Turn In

For this project, you must turn in a brief project report discussing your layout. Specifically, you should describe your approach to the layout, including how you followed "good layout practices" and how you creatively compressed your layout designs to make them small. You must state the geometric sizes (length, width, and area) of both of your designs.

These designs will be graded for

- Meeting given design criteria
- Following good layout practices
- Compactness
- Creativity in the layout

As a result, your layout will be viewed closely. Therefore, you must provide the path to where your layout is stored including your library name/s and cell names. For example, if you have cell called "wrota" that you are turning in for Part 2, and it is in a library called "project7" then you must include in your report and also in the body of an e-mail the complete path name.

~username/Cadence/project7/wrota
~username/Cadence/project7/if_neuron

I will then be able to add this library to my path to then view your layout. Therefore, you do not need to turn in any figures with your report (because I will be directly viewing your layout).