West Virginia University
College of Engineering and Mineral Resources
Lane Department of Computer Science and Electrical Engineering

EE 691W – Data Converter Design

Fall 2013

Class Info

Meeting Time: 5:00-7:20pm
Location: ESB 215
Prerequisites: EE 551
Credit Hours: 3 (Lecture)

Instructor

Dr. David W. Graham
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945 ESB
304-293-9692

Office Hours

10:00-11:00 MW, or by appointment

Text

Required Text
Selected handouts as distributed in class.

Recommended Text
CMOS Analog Circuit Design, Second Edition
Phillip Allen and Douglas Holberg
Oxford University Press, 2002
ISBN: 0195116445

Webpage

www.csee.wvu.edu/~dwgraham/classes/ee691w

Course Description

Design and analysis of data converters. Various topologies of digital-to-analog and analog-to-digital converters are covered, along with critical supporting circuitry such as comparators, switched-capacitor circuits, and sample-and-hold circuits. This course focuses on CMOS technology.

Course Objectives

The purpose of this course is to equip the student with the fundamental concepts of data converter design. At the completion of the course, the student should be able to analyze and design both digital-to-analog and analog-to-digital converters as well as understand the metrics used to characterize their performance. Design will focus primarily on CMOS technology, covering the topics of behavioral modeling, comparators, switched-capacitor circuits, and sample-and-hold circuits along with both Nyquist-rate and oversampled data converters. The student should be able to use theory along with simulation and layout tools to completely design data converters and their supporting circuitry.

Expected Learning Outcomes

1. Ability to analyze and design data converters and supporting circuitry in CMOS technology.
2. Ability to understand the limitations and advantages of different data converter topologies.
3. Ability to analyze and critique publications in the field of data converters.
4. Ability to formulate a design procedure and target specifications for circuit and system applications.
5. Ability to use standard analog circuit computer-aided design (CAD) tools to design digital-to-analog and analog-to-digital converters.

Attendance

Students are responsible for all material covered in class and any announcements made during class time (including changes to test dates, etc.). Please arrive at class on time.

Class Policies
The use of portable phones in the classroom is not permitted (i.e., no calls, no texting, no ringers, etc.). Please remember to turn off your ringers before class. If there are extenuating circumstances that warrant the need of a cell phone in class, let me know *beforehand*.

Assessment

Quizzes	20%
Projects	35%
Final Project	35%
Oral and Written Synopses	10%

Grading A ≥ 90% 90 > B ≥ 80% 80 > C ≥ 70% 70 > D ≥ 60% F < 60%

Reading Assignments
Regular reading assignments will be distributed. These reading assignments must be completed before coming to class, as they will be critical to the class discussion. These reading assignments will cover both traditional data-converter techniques as well as cutting-edge designs from recent publications.

To ensure every student completes the reading assignment before class, a short synopsis of the reading must be turned in at the beginning of the class period in which they are due. Exact details of what is expected for these synopses will be distributed in class.

All students will be required to present a short overview of different reading assignments and lead the discussion on the merits and drawbacks of the circuits under study.

Quizzes
Regular announced quizzes will be given in class to assess understanding of the material covered in class and in the reading assignments. The lowest quiz grade will be dropped.

Projects
Several projects will be assigned to cover the major topics in the class. Approximately one project will be assigned for every major unit of the class. These projects will primarily be design-oriented and will make use of software packages such as MATLAB, SPICE, and circuit layout tools (e.g. Cadence). Not all projects will be of equal value.

Project reports are due at the BEGINNING of class. Late project reports will be deducted by 10 points each twenty-four-hour period after the time in which it is due. Projects turned in after an associated project presentation will be subject to an *additional* 20 point deduction. Additionally, your reports must be turned in electronically via e-mail as well as in paper form. Paper reports *must* be stapled. Detailed directions about the project reports will be provided on the class website.

In addition to the written report, most projects will also require an oral presentation on the due date.

Many of the projects will be done with a partner, and you will turn in a combined report with your partner (you will both receive the same grade). You are *not* permitted to communicate with other groups as you work on these projects.

Short in-class assignments may be given to help aid the discussion and understanding of the material. Any of these that are graded will be included in the Projects portion of the grade.

Final Project
The focus of this class is on the design of data converters. As a result, the Final Project will be a comprehensive design of either an analog-to-digital converter or a digital-to-analog converter. The students will work with the professor to choose a specific topology and appropriate specifications. The students will be required to create a testing plan for the converter along with milestones for the design. In-class design reviews will be conducted, and each student will be able to provide input into other

students' designs. Full transistor simulation and layout will be done. A final presentation of the complete design, along with a detailed report, will be done in the regularly scheduled Final Exam period.

Make-Up Policy
You are expected to attend all quizzes, design reviews, etc. at the scheduled time and location. If you will not be able to attend a class event for a legitimate reason (e.g. religious observance, attending a conference, etc.), let me know within the first week of the semester. Otherwise, you will not be permitted to make them up, unless there is documented proof of urgent medical care or an emergency. Any make up quizzes or projects that are granted may be given as oral examinations, at my discretion.

Honor Code and Academic Honesty Statement
All work you turn in must be completely your own unaided work. I will not tolerate cheating, copying, helping others, or harming others; these are strictly forbidden and are in violation of the university's academic honesty policy, as listed in the undergraduate/graduate catalogs. Plagiarism and any other forms of cheating will be severely penalized and may result in an F grade for the course or receive no credit for the specific test or exam or component of the course. Students are expected to exhibit the same level of professionalism and integrity that will distinguish them in their professional careers. Both the person who reproduced in whole or in any part from the work of others and the person who allowed the work to be copied will be penalized (including partners who turn in joint reports).

(Official University Statement) The integrity of the classes offered by any academic institution solidifies the foundation of its mission and cannot be sacrificed to expediency, ignorance, or blatant fraud. Therefore, I will enforce rigorous standards of academic integrity in all aspects and assignments of this course. For the detailed policy of West Virginia University regarding the definitions of acts considered to fall under academic dishonesty and possible ensuing sanctions, please see the Student Conduct Code at http://studentlife.wvu.edu/studentconductcode.html. Should you have any questions about possibly improper research citations or references, or any other activity that may be interpreted as an attempt at academic dishonesty, please see me *before* the assignment is due to discuss the matter.

Social Justice and Disability Statement
West Virginia University is committed to social justice. I concur with that commitment and expect to foster a nurturing learning environment, based upon open communication, mutual respect, and non-discrimination. Our University does not discriminate on the basis of race, sex, age, disability, veteran status, religion, sexual orientation, color or national origin. Any suggestions as to how to further such a positive and open environment in this class will be appreciated and given serious consideration. If you are a person with a disability and anticipate needing any type of accommodation in order to participate in this class, please advise me and make appropriate arrangements with Disability Services (293-6700).

Disclaimer
The professor reserves the right to make changes in the syllabus. Any changes that are made will be in, what the professor deems, the best interests of the class.

Tentative Schedule
The following is a tentative schedule. The exact schedule, with associated reading assignments, will be kept up to date on the class website. Please complete all reading assignments BEFORE coming to class.

- Unit 1 – Overview of Data Converter Metrics and Specifications (1 week)
- Unit 2 – Behavioral Modeling (1 week)
- Unit 3 – Supporting Circuitry for Data Converters
  - Comparators (1 week)
  - Switched-Capacitor Circuits (2 weeks)
  - Sample-and-Hold Circuits (1 week)
- Unit 4 – Nyquist-Rate Digital-to-Analog Converters (2 weeks)
- Unit 5 – Nyquist-Rate Analog-to-Digital converters (3 weeks)
- Unit 6 – Oversampled Data Converters (2 weeks)
- Unit 9 – Recent Advances in Data Converter Design (2 weeks)