An Ultra-Low-Power Analog Memory System with an Adaptive Sampling Rate

Brandon M. Kelly, Brandon Rumberg, and David W. Graham
Lane Department of Computer Science and Electrical Engineering
West Virginia University, Morgantown, WV 26506
{bkelly6, brumberg}@mix.wvu.edu and david.graham@mail.wvu.edu

***Abstract*—Sleep states are used in resource-constrained systems to conserve power, but they necessitate a wake-up circuit for detecting unpredictable events. In such systems, all information preceding a wake-up event will be forfeited. In this paper, we present an analog memory system that adaptively samples and records an input signal while the rest of the system sleeps, thereby preserving the information that would otherwise be lost. This system does so while consuming less than 3.52 μW. We also show how the adaptive sampling rate can be utilized to approximate the original signal using a minimal number of samples.**

I. Introduction

Wireless sensor networks (WSN) are one type of resource-constrained system that particularly benefit from the use of low-power sleep states. During a sleep state, a device halts normal operation to conserve energy. The device can then be signaled to leave the sleep state by either a wake-up or event-detection circuit so that an interesting event can be observed. The tradeoff faced by designers of WSNs is maximizing the time a node spends in the sleep state to conserve power while minimizing the number of events that the node misses.

Many techniques exist to optimize the duty cycles of WSNs and ensure that interesting events are not missed by the sensor nodes [1]–[5]. However, all of these techniques entail the possibility of losing some interesting data just before the event occurs or during the moment between the detection of the event and the node fully waking up. For applications where the prelude to an event may contain valuable information, a memory buffer must be included to continuously record the data before an event is detected.

While a digital memory buffer could be implemented in a WSN node to record the input during a sleep state, its use would negate much of the power savings garnered by the use of sleep states. A digital memory buffer's storage process involves reading samples through an analog-to-digital converter and then storing the values in some type of digital memory. The sampling rate needs to be at least the Nyquist rate of the highest frequency component of the signal in order to preserve the information contained in the signal. Continuous sampling at such a high rate is costly in terms of both power consumption and real estate (i.e., area required for storing the sequence of digital values). These drawbacks make digital memory buffers undesirable for applications in which ultra-low-power operation is a necessity.

This work was supported in part by the United States Army Research Laboratory under Contract W911NF-10-2-0109.

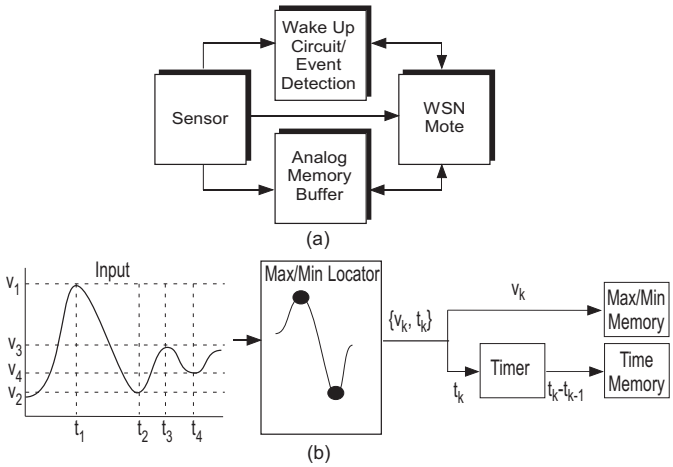

Fig. 1. (a) To avoid the data loss normally associated with sleep states in WSNs, we introduce an ultra-low-power analog memory buffer to operate in parallel with a wake-up circuit. This system records data from the sensor while the WSN mote is allowed to remain in a sleep state, enabling signal approximation without sacrificing the energy savings from the sleep state. (b) Our analog memory buffer locates the local maxima and minima in real time and stores their respective amplitudes and times separately.

In this paper, we propose an ultra-low-power analog memory system that asynchronously samples a signal and then stores those samples in a buffer. This system operates in parallel with a wake-up circuit (Fig. 1(a)) to store signal information while the rest of the system sleeps. To further reduce the power consumption and size of the analog buffer, we minimize the number of required samples by recording only the local maxima and minima of the signal. This novel approach effectively adapts the sampling rate to the instantaneous Nyquist rate of the signal, thereby minimizing the number of samples needed for accurate reconstruction. We also demonstrate a simple, yet powerful, technique for approximating the original signal using only max/min values. Unless otherwise noted, all plots in this paper are measured results from our memory system which was fabricated in a 0.5μm standard CMOS process available through MOSIS.

II. System Overview

Traditional Nyquist sampling of a signal necessitates sampling at a frequency greater than twice the highest frequency

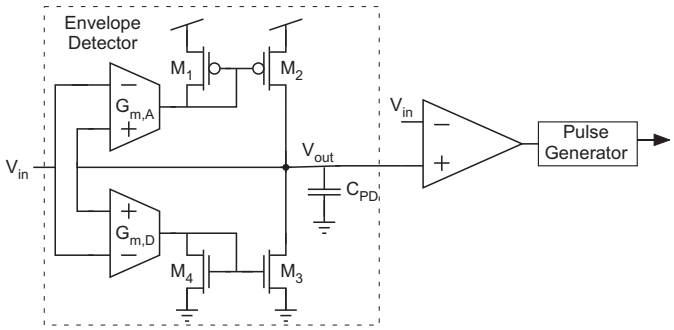

Fig. 2. The maximum locator circuit consists of an envelope detector, a comparator, and a pulse-generation circuit. The envelope detector tracks the input on the rising slope of the signal and then slowly decays on the falling slope of the input signal. This tempered decay rate causes the comparator to detect a discrepancy at the point when the signal begins to decay, i.e. the local maximum. The comparator then signals a pulse generator, which triggers the write phase in the memory storage unit. The minimum locator circuit operates similarly, tracking the input on the falling slope and lagging the input on the rising slope.

component of the original signal. Using this constant rate of sampling leads to oversampling when the signal does not contain the highest allowable frequency components [6]. Wasting system resources on superfluous samples is a primary source of inefficiency in memory buffers.

A system designed for minimal power consumption should be able to adapt in real time to the changing frequency of the signal being sampled to avoid resource inefficiency. In this work, we suggest that sampling only the local maxima and minima (both amplitude and time) provides sufficient information about a time varying signal to produce an adequate approximation. Recording only max/min values, for a properly bandlimited signal, yields a sampling rate that adjusts dynamically to the instantaneous Nyquist rate. We note that scheduled wake-up cycles are adequate for sampling slowly varying signals and DC levels, while still maintaining low-power performance. Therefore, we focused our device on time varying (AC) signals.

Max/min sampling is achieved through the use of a multi-stage analog system (Fig. 1(b)). When a local max/min is detected, its voltage value and the time since the last max/min are stored in an analog memory buffer. These values can then be accessed later for reconstruction or for further analysis.

Within our analog memory system, the max/min locator generates a pulse when the signal needs to be sampled. This pulse enables the write phase in two different analog memory storage units, which are implemented as an array of sample-and-hold circuits. This write pulse causes the memory units to record the voltage value as well as the time since the previous max/min. This sampling scheme results in a series of voltage-time pairs that can be used to approximate the original signal.

III. Subsytem Implementations

In the following subsections, we discuss each of the circuits used to create the analog memory system.

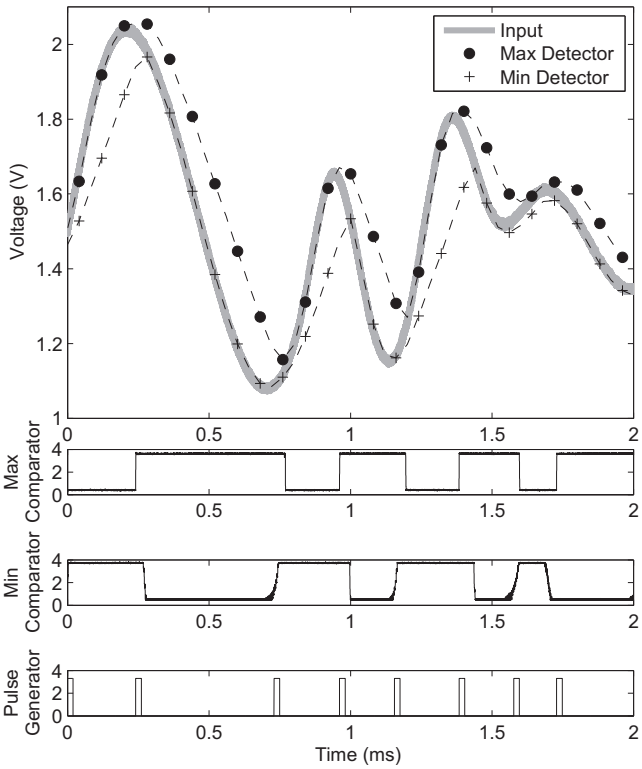

Fig. 3. The max/min locator circuits operate by tracking the input on the rising/falling slope, and then decaying at a slower rate. The descrepency between the decay of the max/min locator circuit and the original signal is detected by the comparator, which in turn signals the pulse generator to activate a write pulse.

A. Max/Min Locator

The max/min locator circuit is used to trigger the write phase in the short-term memory, so that only maxima and minima are sampled. Detection of local maxima and minima is achieved through the use of symmetric max/min locator circuits operating in parallel. Because of this symmetry, we will only discuss the maximum locator.

The core of the maximum locator circuit is the envelope detector (Fig. 2), which we introduced in [7]. A pair of transconductors compare V_{out}, the value stored on the capacitor by the envelope detector, with V_{in}, the system input. When V_{in}>V_{out}, the top path is active and the capacitor is charging; otherwise, the bottom path is active and the capacitor is discharging. By biasing $G_{m,A}$ such that $G_{m,A}/C_{PD}$ is at least on the order of the signal frequency, V_{out} will track V_{in} up to the local maximum. Then, by using a weaker biasing for $G_{m,D}$, V_{out} will begin to lag behind V_{in} as the signal decays.

The operation of the on-chip max/min locator can be seen in the top pane of Fig. 3. When V_{out} lags V_{in}, the comparators of the max/min locator circuits produce an output of logic high. On the rising edge of the output of either comparator, the pulse generator signals the memory system to enter the write phase and sample the input (Fig. 3).

For flexibility in defining the timing of the pulse generator and memory addressing, we implemented the pulse gener-

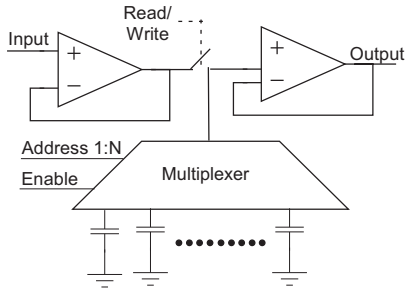

Fig. 4. The capacitor bank tracks the system input and enters write operation only when the max/min locator's pulse generator outputs a logic high signal. After each write, the address of the selected capacitor is incremented through the break-before-make multiplexer.

ator using an off-chip complex programmable logic device (CPLD). In a subsequent version of this system, the CPLD functionality will be integrated with the rest of the system.

B. Short-Term Memory

The short-term memory subsystem records the amplitude of the input wave at the time of max/min detection. The memory subsystem is formed by a 64-element array of sample-and-hold circuits that are accessed through a break-before-make muliplexer (Fig. 4). Read and write operation is controlled by the pulses received from the max/min locator circuit. The memory system continuously loops through the capacitors until a wake-up event has been detected and the samples need to be read. The hold time of the storage capacitors is limited by the leakage through the reverse-biased p-n junctions in the transmission gate switches; this hold time can be specified by proper sizing of the capacitors at design time.

C. Timing Circuit

The timing circuit utilized by this system is a capacitive time-to-voltage converter. After each max/min is found, the capacitor is set to a known value and is then charged by a constant current source. Then, when the next max/min is found, the capacitor's voltage is sampled and stored in the same manner as the max/min voltages. The stored voltage, along with the known charging rate for the capacitor, can be used to calculate the time between maxima and minima.

IV. System Examples

To demonstrate the range of operation of this analog memory buffer, several input signals were analyzed with a single set of bias points. While the system's biasing can be adapted to capture a large range of signals, this section will focus on the capability of the system for a single biasing condition.

These demonstration system tests were performed using the on-chip max/min locator, while the timing, pulse generation, and storage components were performed using MATLAB. The outputs of the on-chip max/min locator were obtained via a data acquisition board. While the storage and timing components were fabricated and verified through simulation and/or testing, we chose to use MATLAB to emulate them instead. Utilizing these devices would have required compensation for charge leakage and sharing. While these components are important, they primarily provide timing or holding of values; thus, using idealized MATLAB functions to represent them more clearly demonstrates the performance of the max/min locator, which is the core of the analog memory buffer and the associated algorithm.

The max/min locator was found to operate on signals with amplitudes ranging from 30mV$_{pp}$ to 1.5V$_{pp}$ and on signals with frequencies ranging from 30Hz to 30kHz. Figure 5(a)-(b) demonstrates finding max/min locations on an AM modulated waveform as well as on a chirp signal.

The system was also shown to reliably capture the local maxima and minima of a voice signal. Figure 5(c)-(d) shows that that the majority of the wave was well approximated. Error found in the approximation of the original signal results from two sources. The first occurs from portions of the signal that are not properly bandlimited. We plan to correct this issue in future iterations by performing a filtering operation to remove high-order harmonics and high-frequency noise before attempting max/min location. The second source of error occurs when a small max (min) follows a large max (min) too closely in time. In this case, the max/min locator is unable to decay quickly enough to resume tracking the signal in time for max/min detection. For these few portions of the signal, we are undersampling and cannot recreate the waveform exactly. However, we note that the speech signal that was reconstructed from the measured max/min values was intelligible, with low perceived distortion, even in the presence of these two types of sampling errors.

The reconstruction of the 1.68s speech sample demonstrated adequate approximation using a minimal amount of resources. In total, 652 samples were recorded, and the highest frequency captured was 3125Hz. If a constant-sampling-rate technique were used, a sampling frequency of 6250Hz would be necessary, and a total of 10556 samples would have to be recorded. In addition to the 16-fold savings in sample storage afforded by the adapted sampling rate, the system had low power consumption: 1.17μW for the max/min locator and 0.586μW for each of the four buffers used in the storage system combine for a total power consumption of 3.52μW. These power consumptions were simulated because we were unable to access individual components on chip.

The signals were reconstructed using a simple, yet powerful, interpretation of the Bézier curve formula [8] given by:

$$\begin{aligned} B(x) =&(1-x)^3P_0 + 3(1-x)^2xP_1 \\ &+ 3(1-x)x^2P_2 + x^3P_3, \quad x \in [0,1] \end{aligned} \tag{1}$$

The Bézier curve formula generates points along a smooth curve that is specified by the endpoints, P_0 (at x=0) and P_3 (at x=1), and concavity points, P_1 and P_2. We utilize the formula sample-by-sample to interpolate between every pair of adjacent max/min values. Thus, we take N max/min samples and generate $N-1$ segments between them to create a full approximation of the signal. For each segment, the formula is applied to the voltage and time values separately. By understanding that all sample values are located where the derivative

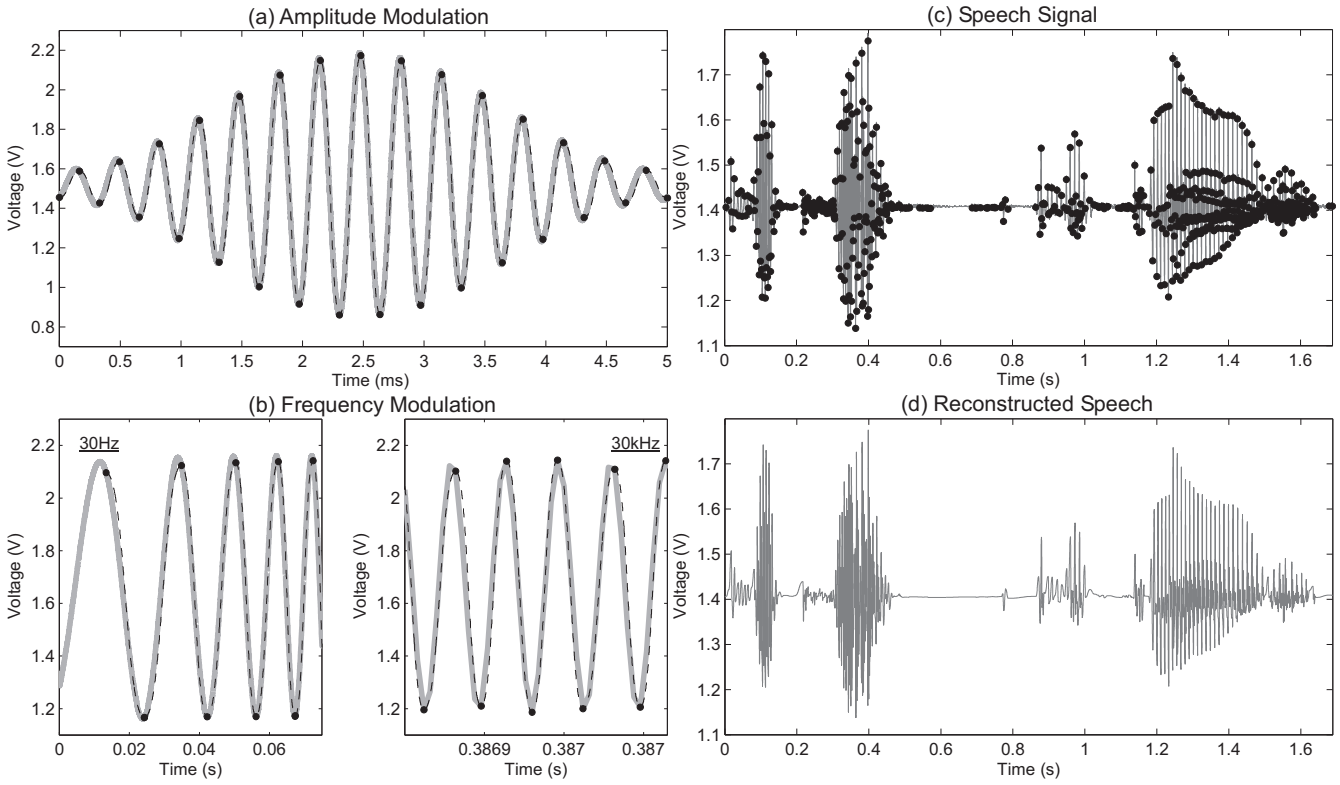

Fig. 5. (a-b) The system is capable of capturing a wide range of amplitudes and frequencies. For these plots, the input is shown in grey, detected max/mins are black dots, and the reconstructed wave is a black dashed line. (c) The speech clip used as input to the system is shown in grey with detected max/mins in black dots. (d) The speech clip approximation from using the modified Bézier formula with the sampled max/mins.

of the input equals zero (i.e., where the slope is zero), the Bézier formula can be simplified by setting the points P_1 and P_2 to be equal to the max/min locations. Accordingly, the equation for interpolating the voltage between samples $k-1$ and k is

$$\begin{aligned} V(x) =&(1-x)^3V_k + 3(1-x)^2xV_k \\ &+ 3(1-x)x^2V_{k-1} + x^3V_{k-1} \end{aligned} \quad (2)$$

The result of this equation is a nearly sinusoidal-shaped curve that spans the specified amplitudes. The time vector is interpolated similarly, except that the concavity points are set to the midpoint of the time interval T_{kmid}= (T_k+T_{k-1})/2, as

$$\begin{aligned} T(x) =&(1-x)^3T_k + 3(1-x)^2xT_{kmid} \\ &+ 3(1-x)x^2T_{kmid} + x^3T_{k-1} \end{aligned} \quad (3)$$

The result is a vector of time values that shift the sinusoidal curve to the appropriate time endpoints.

We have found the Bézier equation to be a promising method for reconstructing a signal from its max/min values, as indicated by Fig. 5. By further fine tuning this method, and by improving our current subsystem implementations, we hope to increase the range of signals that we are able to recreate.

V. Conclusion

We have presented a low-power system capable of recording and reconstructing a pre-defined duration of a signal, prior to the wake-up event of an embedded system. The system was shown to faithfully recreate a variety of waveforms. Operation across a range of amplitudes and frequencies was demonstrated, as was application upon a voice signal.

References

[1] M. Malinowski, M. Moskwa, M. Feldmeier, M. Laibowitz, and J. Paradiso, "Cargonet: A low-cost micropower sensor node exploiting quasi-passive wakeup for adaptive asynchronous monioring of exceptional events," in *ACM Sensys*, 2007.

[2] B. Rumberg, D. Graham, V. Kulathumani, and R. Fernandez, "Hibernets: Energy-efficient sensor networks using analog signal processing," *IEEE J. Emerging and Selected Topics in Circuits and Systems*, vol. 1, no. 3, pp. 321–334, Sept. 2011.

[3] S. Jevtic, M. Kotowsky, R. Dick, P. Dinda, and C. Dowding, "Lucid dreaming: Reliable analog event detection for energy-constrained applications," in *Proc. Info. Processing in Sensor Networks*, 2007, pp. 350–359.

[4] D. Goldberg, A. Andreou, P. Julián, P. Pouliquen, L. Riddle, and R. Rosasco, "A wake-up detector for an acoustic surveillance sensor network: Algorithm and VLSI implementation," in *Proc. Info. Processing in Sensor Networks*, 2007, pp. 134–141.

[5] P. Dutta, M. Grimmer, A. Arora, S. Bibyk, and D. Culler, "Design of a wireless sensor network platform for detecting rare, random, and ephemeral events," in *Proc. Info. Processing in Sensor Networks*, 2005.

[6] D. Wei and A. Oppenheim, "Sampling based on local bandwidth," in *Asilomar Conference on Signals, Systems, and Computers*, Nov. 2007, pp. 1103–1107.

[7] B. Rumberg and D. Graham, "A low-power magnitude detector for analysis of transient-rich signals," *IEEE J. Solid-State Circuits*, vol. 47, no. 3, pp. 676–685, March 2012.

[8] G. Farin, *Curves and Surfaces for CAGD: A Practical Guide*. Academic Press, 1996.