An Asynchronous ADC with Reconfigurable Analog Pre-Processing

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***Abstract*—Many energy constrained devices such as cell-phones and wearable medical devices utilize sparse or bursty signals—signals characterized by relatively short periods of high activity. Traditional Nyquist-Rate converters are an inefficient tool for converting sparse signals, as a great deal of energy is wasted converting portions of the signal with relatively-low information content. Asynchronous sampling methods attempt to circumvent this inefficiency by sampling based upon the characteristics of the signal itself. However, many asynchronous sampling solutions struggle with a robustness/resolution trade-off. In this paper, we present a new paradigm in which a flexible analog front-end is paired with an asynchronous successive approximation data converter and an asynchronous time-to-digital converter. The result of this paradigm is that the system can be adapted to individual applications, allowing specific data points to be targeted and avoiding data conversion inefficiency. The system will be demonstrated along with the example application of measuring the QRS-complex within an ECG waveform. The demonstrated system, fabricated in standard 0.5μm and 0.35μm processes, produces a minimal number of voltage/time pairs required for studying the QRS complex while consuming 5.96μW of static power.**

I. Introduction

Passive voice monitoring in cell-phones, wearable bio-medical devices, and a variety of other modern systems bear a common burden—monitoring sparse or bursty signals in a resource constrained environment. Sparse signals undergo short periods of high activity among longer periods of relative inactivity. This sporadic data content makes traditional analog-to-digital conversion using Nyquist-Rate sampling inefficient because the conversion of unnecessary or uneventful data yields little information. Such data-conversion inefficiency greatly impacts the overall power-budget of the system and is a key hurdle in enabling usability and proliferation of such energy-constrained devices.

Some data converters attempt to vary their sampling rate based upon the spectral content of the target signal. One of the more popular data-driven designs is the level-crossing ADC (e.g. [1]). Level-crossing ADCs require a number of threshold levels proportional to the desired resolution, but as the number of levels is increased, the bandwidth of the signal becomes limited. The work in [2] addressed this bandwidth issue by adapting the level spacing to the changing frequency content of the signal. But, in addition to the increased digital overhead, there is still the possibility of taking superfluous samples which yield no new or useful data. A potentially improved method would be to use analog pre-processing to identify specific portions of the signal which contain relevant data, while disregarding the other portions of the signal.

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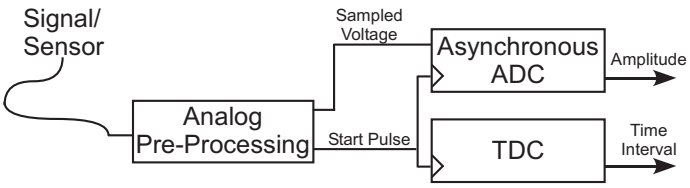

Fig. 1. Asynchronous analog-to-digital conversion system. A reconfigurable analog front end reduces information to only the relevant data points and also triggers the subsequent blocks which then produce digital words for the corresponding voltages and time intervals.

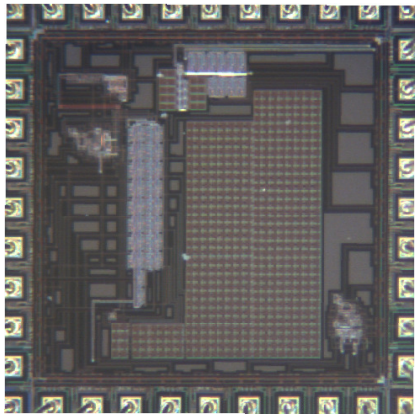

Fig. 2. Die photograph of the asynchronous ADC/TDC fabricated in a 0.5μm standard CMOS process available through MOSIS.

In this paper, we propose an asynchronous sampling system which can be tuned for a variety of applications. The sampling system produces two digital signals—one proportional to the sample amplitude and the other proportional to the inter-sample time period [Fig. 1]. The trigger mechanism for these data-driven asynchronous measurements is controlled by an analog front-end implemented in our reconfigurable analog/mixed-signal platform (RAMP) system [3]. The use of a reconfigurable front-end allows us to create a sample triggering mechanism tuned to the minimal amount of required data. The well-tuned analog front-end combined with asynchronous data conversion allows for highly efficient data extraction.

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The system presented here samples based upon the extrema-sampling paradigm which has been explored in [4], [5], but this system could be used with a variety of sampling methods, particularly for well understood and characterized signals. Section II establishes the overall system architecture which we used to implement this adaptive sampling technique. The individual components of the system are then examined in Section III. Finally, Section IV concludes with an example usage of the system in an electrocardiogram (ECG) monitoring environment. Unless otherwise noted, all plots in this paper are measured results from the ADC/TDC which was fabricated in a 0.5μm standard CMOS process [Fig. 2] or from the RAMP system [3] fabricated in a 0.35μm standard CMOS process all available through MOSIS.

II. System Overview

When sampling signals with sparse information, constant-rate sampling unavoidably creates extraneous samples during periods of low activity. Such inefficiency can be avoided by the use of analog pre-processing, which has been shown to be computationally efficient [6]. While a fully custom front-end would yield the highest energy savings, the use of the RAMP reconfigurable platform [3] allows us to adapt this analog front-end for a variety of applications. Many sampling paradigms could be used with this system, and we have chosen to demonstrate this system using extrema sampling.

The RAMP system identifies and samples the extrema values in a manner similar to that proposed in [4], locating the local minimums and maximums with two symmetric extrema detection and sampling circuits. For some applications, the extrema amplitude values and inter-sample time values are enough to extract useful information. By performing the identification of these values in the analog domain, it is possible to leave the data converter inactive until an appropriate value has been sampled.

Once an extrema value has been sampled, the ADC/TDC are signaled and begin their respective conversions. The ADC utilizes a simple successive approximation architecture. The TDC is essentially a voltage-controlled oscillator with a digital counter attached to the output that counts the number of oscillations between extrema occurrences. By holding the voltage-bias constant and pausing/resetting the TDC after every sample, the total number of counted oscillations will be proportional to the elapsed time since the previous sample, thus enabling inter-sample time measurement.

III. Subsystem Implementations

Below, we detail the individual components that create the asynchronous sampling data converter.

A. Analog Front End for Pre-Processing

Locating and sampling the extrema values of the signal was performed by an analog front end [Fig. 3] implemented within the reconfigurable analog RAMP system [3]. The RAMP system allows the user to specify different configurations of analog (filters, envelope detectors, multipliers, etc.) and digital components in a manner similar to operating an FPGA.

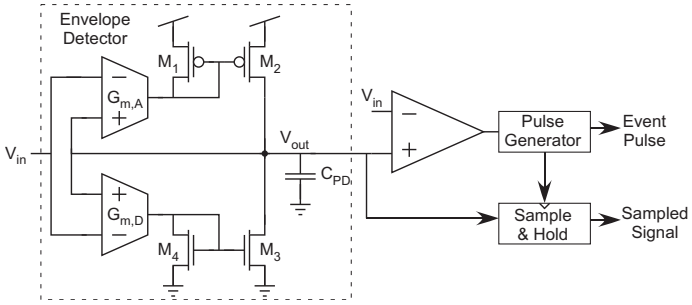

Fig. 3. The maximum locator circuit which makes up one half of the analog front end synthesized in the RAMP system. The circuit consists of an envelope detector, a comparator, a pulse-generation circuit, and a sample-and-hold. The envelope detector tracks the input on the rising slope of the signal and then slowly decays on the falling slope of the input signal. This lagging decay is detected by the comparator—signaling a local maximum. The comparison signal is then converted into a pulse which triggers both the sample-and-hold circuit as well as the subsequent ADC/TDC stages. The minimum locator circuit is the symmetric equivalent, tracking the input on the falling slope and lagging the input on the rising slope.

Locating the maximum extrema of the signal was performed by first taking the envelope of the signal. This envelope was set to track the input aggressively on the rising edges and to lag behind when the signal began to decline. The comparator then produced a logic high signal when the envelope lagged behind the input. This logic high value was used to trigger a pulse generator which provided the 'event pulse' signal. In addition to signaling the subsequent data converter stages, the pulse also triggered a sample-and-hold circuit which sampled the value of the input. All of these circuits were implemented on the RAMP. The sample was then provided to the data converter. The minimum extrema location was performed with a symmetrically equivalent circuit.

B. Successive-Approximation ADC

The amplitude conversion of the extrema values was performed by a successive approximation ADC. The successive approximation architecture was chosen for its demonstrated power efficiency [7]. It also has the advantage of being appropriate for a relatively large range of frequencies and amplitudes, thus making it an appropriate choice for a variety of different systems with varying signal characteristics.

Maximizing resources within energy-constrained systems is a high priority, but it is difficult, for example, to convert voltages along the entire full-scale range. The comparator shown in Fig. 4 was based on the design in [8] and was modified to maximize system resources by enabling rail-to-rail conversion. Normally, a comparator is implemented with either a pFET-based differential pair, which suffers at higher voltages, or an nFET-based differential pair, which suffers at lower voltages. Ours uses both complimentary versions of the pFET-based and nFET-based comparators and selects which one to use based upon the result of the first successive approximation.

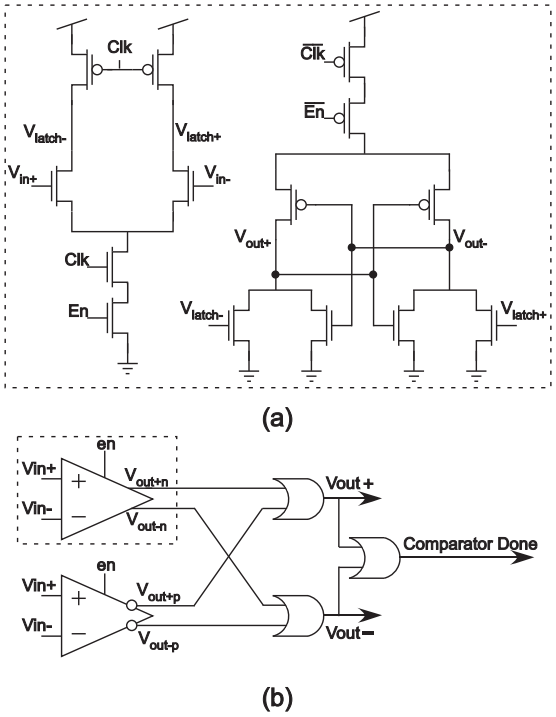

Fig. 4. Comparator schematics. (a) The clocked comparator is designed to use negligible static energy and very little dynamic energy by utilizing minimally sized transistors. Prior to comparison, the clock signal is low, which pre-charges the V_{latch} nodes. When the clock goes high, the V_{latch} nodes are discharged at rates proportional to the V_{in+} and V_{in-}. These V_{latch} nodes control the subsequent voltage latch stage. The end result is that the output node that corresponds to the higher input voltage will be pulled high. (b) The nFET-comparator is paired with its pFET equivalent. The appropriate comparator is chosen by the MSB of the successive approximation register, thus ensuring that the comparator never operates in a region where it cannot make an accurate comparison. These outputs are then OR'd together to create a comparator done signal.

During the first successive approximation, it is already known that one of the comparator inputs will be at the mid-rail voltage. Therefore, either a pFET-based or nFET-based comparator would be able to perform the comparison. We chose the nFET-based version to perform the first conversion. The result of this conversion signifies whether the input is in the top-half or bottom-half of the full scale range. If it is found to be in the top-half, we perform the remaining conversions using the nFET-based comparator. Conversely, if the input is found to be in the bottom-half, the remainder of the conversion is performed using the pFET-based comparator. By intelligently selecting which comparator is used, we are able to convert values along the entire full-scale range.

Once the appropriate input pair is selected, the matched FETs conduct at a rate proportional to the input voltages applied to their gates. The nodes that are discharged by these FETs are attached to a clocked latch which cause one output node to become logic high while the other output node becomes logic low. The result signifies which voltage input was greater.

The drawback to using two symmetric comparators is that two different input-referred offsets must be accounted for in post-processing. For this implementation, no layout matching techniques were used to address this unequal offset, but it would be a viable technique for mitigating the issue. Another method would be to use programmable floating-gate devices in place of the input pairs. The floating gates could then be programmed with the appropriate charge so that the offsets between the two halves of the comparator matched [9].

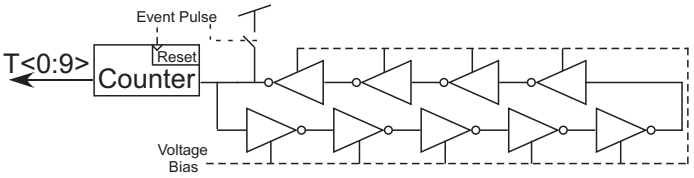

Fig. 5. Time-to-digital converter consisting of a voltage-controlled oscillator and a counter. The counter keeps track of the number of oscillations. The resulting digital word is proportional to the time elapsed since the last event pulse. The event pulse clears the counter and also shorts part of the oscillator to logic high, which ensures that it begins in the same state after every reset.

C. Time-to-Digital Converter

The inter-sample times are recorded using a time-to-digital converter (TDC). A time-to-digital converter is simply a device which takes some periodic or known signal and uses it to estimate the time interval between signal pulses [10].

Our TDC implementation was designed to take a minimal amount of room and a minimal amount of digital support circuitry. The periodic signal was created by current-starved inverters arranged in a voltage-controlled oscillator topology [Fig. 5]. The current starving ensured that we could both mitigate the power wasted by short-circuit current and that we could control the frequency of oscillation of the overall device. The voltage bias was held at a DC value and the output oscillations were recorded using a digital counter. The output of this counter was then a binary word which was proportional to the length of time since the last restart pulse. The restart pulse was provided by the RAMP system and was used to reset the counter values to zero when a new sample was detected.

IV. System Example

To illustrate the functionality of the asynchronous ADC architecture with real-world signals, we created a simple electrocardiogram (ECG) monitoring system. ECG waveforms are very well understood signals which have a limited number of medically relevant data points. Our example will focus on QRS-complex capture, disregarding the other portions of the ECG wave. QRS-complexes are useful for a variety of medical purposes ranging from monitoring for hyperkalemia or cardiac hypertrophy to simply extracting heart-beat to estimate perceived exertion [11]. For the purpose of demonstrating this system, an extrema sampling approach is a natural fit for reducing an ECG waveform to its QRS-complex—which can be viewed as a distinct local maximum between two local minima. By extracting only the QRS-complex and avoiding sampling extraneous data, this device would allow a wearable health or fitness system to be a more viable long-term option. The relevant performance metrics for this example are summarized in Table I.

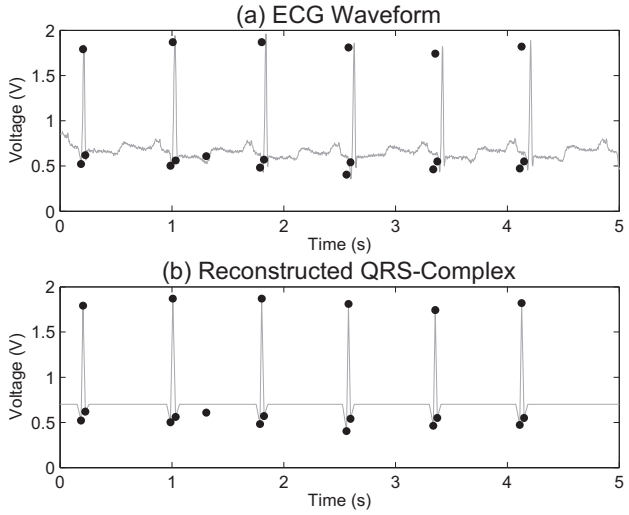

Fig. 6. (a) The original ECG waveform (gray line), taken from the MIT arrhythmia database, with the detected extrema values (black). While the period-to-period temporal accuracy is relatively high, error aggregates creating the appearance of a shorter signal. This aggregate error could be addressed in post-processing. (b) QRS-complex reconstruction (gray) with the detected QRS values (black) as well as a single false positive.

The first task in implementing a QRS-complex monitoring system is identifying and sampling the QRS peaks. By performing this pre-processing in the analog domain, we can save a great deal of power. Figure 6 shows the operation of the system and the resultant approximations of the amplitudes and time intervals between the QRS peaks. The device was tested with real world data taken from the MIT arrhythmia database [12] and had a measured static power consumption of 4.95μW.

When the analog front-end signals the occurrence of a QRS extrema, the TDC halts operation, allowing readout of the digital word which represents the time duration since the previous extrema occurrence. The TDC is then reset, allowing it to begin counting up until the next extrema occurrence. The TDC can operate with frequencies ranging up to tens of kilohertz, but for this particular test, the TDC was operated at a frequency of 1.15kHz for a measured power consumption of 1.01μW. It should be noted that this component will greatly benefit from smaller fabrication processes and lower power supplies.

The analog front-end also simultaneously signals the ADC to begin converting the newly sampled extrema. The ADC has an extremely low static current draw measured at 14.75nW. The low static-current means that the ADC can remain powered on between samples without worry of draining the power budget. The simulated energy per conversion was 47.4nJ.

In viewing the operation of the entire system, the advantages of adaptive sampling become readily apparent. Figure 6 shows the system effectively capturing a QRS-complex. The highest frequency component, which is the change between Q and R, would determine the minimum sampling rate in a traditional Nyquist sampling scheme. For the demonstrated waveform, the 57Hz change would necessitate a sampling rate of 114Hz from a conventional Nyquist-rate ADC. This sampling rate would yield approximately 485 samples over the 4.228 seconds that the signal is demonstrated over. That amount of extra needless samples is greater than 25 times the number of samples taken in our system, even including the single false-positive.

TABLE I
TABLE OF PERFORMANCE

Analog Front End -QRS Monitoring	Power Consumption: 4.95μW
ADC -QRS Voltage Values	Resolution: 8-bits Static Power: 14.75nW Energy per Conversion: 47.4nJ
TDC -QRS Timing Values	Resolution: 10-bits Power Consumption: 1.01μW

V. CONCLUSIONS

We have presented a system capable of converting well-understood signals asynchronously and at a low-power cost. The samples were in the form of voltage/time pairs and allow valuable information to be taken from the signals with minimal energy expenditure. The system was demonstrated on real-world ECG signals and was shown to faithfully capture the QRS-complexes. We plan to extend this system past the extrema-sample paradigm to include other event-driven applications including voice-detection and gait detection.

REFERENCES

[1] K. Kozmin, J. Johansson, and J. Delsing, "Level-crossing ADC performance evaluation toward ultrasound application," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 56, no. 8, pp. 1708–1719, Aug 2009.

[2] M. Trakimas and S. Sonkusale, "An adaptive resolution asynchronous ADC architecture for data compression in energy constrained sensing applications," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 58, no. 5, pp. 921–934, May 2011.

[3] B. Rumberg, D. Graham, S. Clites, B. Kelly, M. Navidi, A. Dilello, and V. Kulathumani, "RAMP: Accelerating wireless sensor hardware design with a reconfigurable analog/mixed-signal platform," in *Proc. of ACM/IEEE Inform. Process. in Sensor Networks*, 2015, pp. 47–58.

[4] B. Kelly, B. Rumberg, and D. Graham, "An ultra-low-power analog memory system with an adaptive sampling rate," in *Proc. of IEEE MWSCAS*, Aug. 2012, pp. 302–305.

[5] D. Rzepka and M. Miskowicz, "Recovery of varying-bandwidth signal from samples of its extrema," in *Signal Processing: Algorithms, Architectures, Arrangements, and Applications*, Sept. 2013, pp. 143–148.

[6] R. Sarpeshkar, "Analog versus digital: extrapolating from electronics to neurobiology," *Neural computation*, vol. 10, no. 7, pp. 1601–1638, 1998.

[7] B. Jonsson, "An empirical approach to finding energy efficient ADC architectures," in *Proc. of 2011 IMEKO IWADC & IEEE ADC Forum*, 2011, pp. 1–6.

[8] D. Schinkel, E. Mensink, E. Klumperink, E. van Tuijl, and B. Nauta, "A double-tail latch-type voltage sense amplifier with 18ps setup+hold time," in *Proc. of IEEE ISSCC*, Feb. 2007, pp. 314–605.

[9] F. Adil, G. Serrano, and P. Hasler, "Offset removal using floating-gate circuits for mixed-signal systems," in *Proc. of Southwest Symposium on Mixed-Signal Design*, Feb. 2003, pp. 190–195.

[10] G. Roberts and M. Ali-Bakhshian, "A brief introduction to time-to-digital and digital-to-time converters," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 57, no. 3, pp. 153–157, March 2010.

[11] H. Yoo and C. van Hoof, *Bio-Medical CMOS ICs*. Springer, 2010.

[12] A. L. Goldberger *et al.*, "PhysioBank, PhysioToolkit, and PhysioNet: Components of a new research resource for complex physiologic signals," *Circulation*, vol. 101, no. 23, pp. e215–e220, 2000.