A FIVE-TRANSISTOR BANDPASS FILTER ELEMENT

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ABSTRACT

This paper explores a five-transistor continuous-time band-pass filter element called the Capacitively Coupled Current Conveyer (C^4) with a programmable pass-band. We show measurement data from 1Hz to 100kHz . This paper discusses the effects of various design parameters on frequency-range, gain and linearity. Experimental data is presented from circuits fabricated on a 0.5μm nwell CMOS process available through MOSIS.

Band-pass filter elements have a long history, from simple linear-systems to standard implementations [1]. The main use being some form of signal decomposition, whether it be to amplify/attenuate a specific signal frequency, or to separate multiple frequencies [2, 3, 4]. Tuning of these devices is critical [5, 6], in addition to matching, power, and overall die area. The filter discussed in this paper has a simple topology (5 transistors), uses a single power-supply, uses very little power, and is easily tunable. It will also serve as a good starting point for developing higher order bandpass filters.

The initial theory on the capacitively coupled current conveyer (C^4) was developed from the Autozeroing Floating-Gate Amplifier (AFGA) [7], which had widely separated corner frequencies due to limitations of the device. The C^4 is a capacitively based bandpass filter that models the tunneling and the hot-electron injection with transistors, thus removing the corner frequency limitations. The circuit is shown in Fig. 1. This circuit has previously been used in many systems [8, 4], but these applications were designed with very low Q's, typically less than 1. Such low values of Q will not work for some applications, one example of this would be a cochlea stage which requires Q's as high as 30 for low amplitude signals. In designing systems with moderate to high Q's there are certain properties that will play a significant role. Within this paper, we hope to cover these issues to clarify the design and use of the C^4 within these systems.

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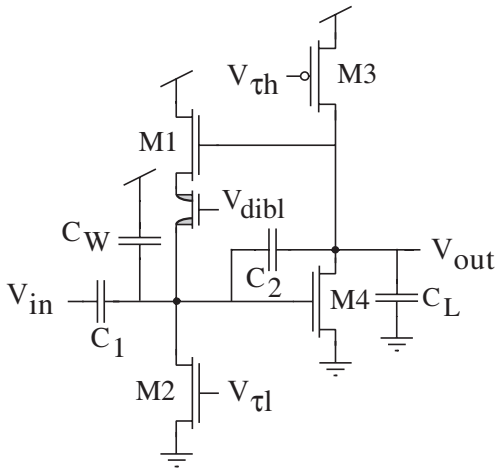

Fig. 1. Schematic of a single C^4 structure. The capacitors model all explicit and parasitic capacitances in the signal path of the circuit.

1. FREQUENCY TUNING

The C^4's corner frequencies are electronically tunable and can be set independently of one another. The frequency response of the C^4 is governed by

$$\frac{V_{out}}{V_{in}} = -\frac{C_1}{C_2}\frac{s\tau_l(1-s\tau_f)}{s^2\tau_h\tau_l + s(\tau_l + \tau_f(\frac{C_o}{\kappa C_2} - 1)) + 1} \quad (1)$$

where the time constants are given by

$$\tau_l = \frac{C_2 U_T}{\kappa I_{\tau_l}} \qquad \tau_f = \frac{C_2 U_T}{\kappa I_{\tau_h}}$$
$$\tau_h = \frac{C_T C_O - C_2^2}{C_2}\frac{U_T}{\kappa I_{\tau_h}}$$

U_T is the thermal voltage ($25.9mV@25^oC$) and κ is the subthreshold slope. The total capacitance, C_T, and the output capacitance, C_O, are defined as $C_T = C_1 + C_2 + C_W$ and $C_O = C_2 + C_L$. The currents I_{τ_l} and I_{τ_h} are the currents through M_2 and M_3, respectively in Fig. 1. With normal usage, τ_f is so fast that the zero it produces lies far out-

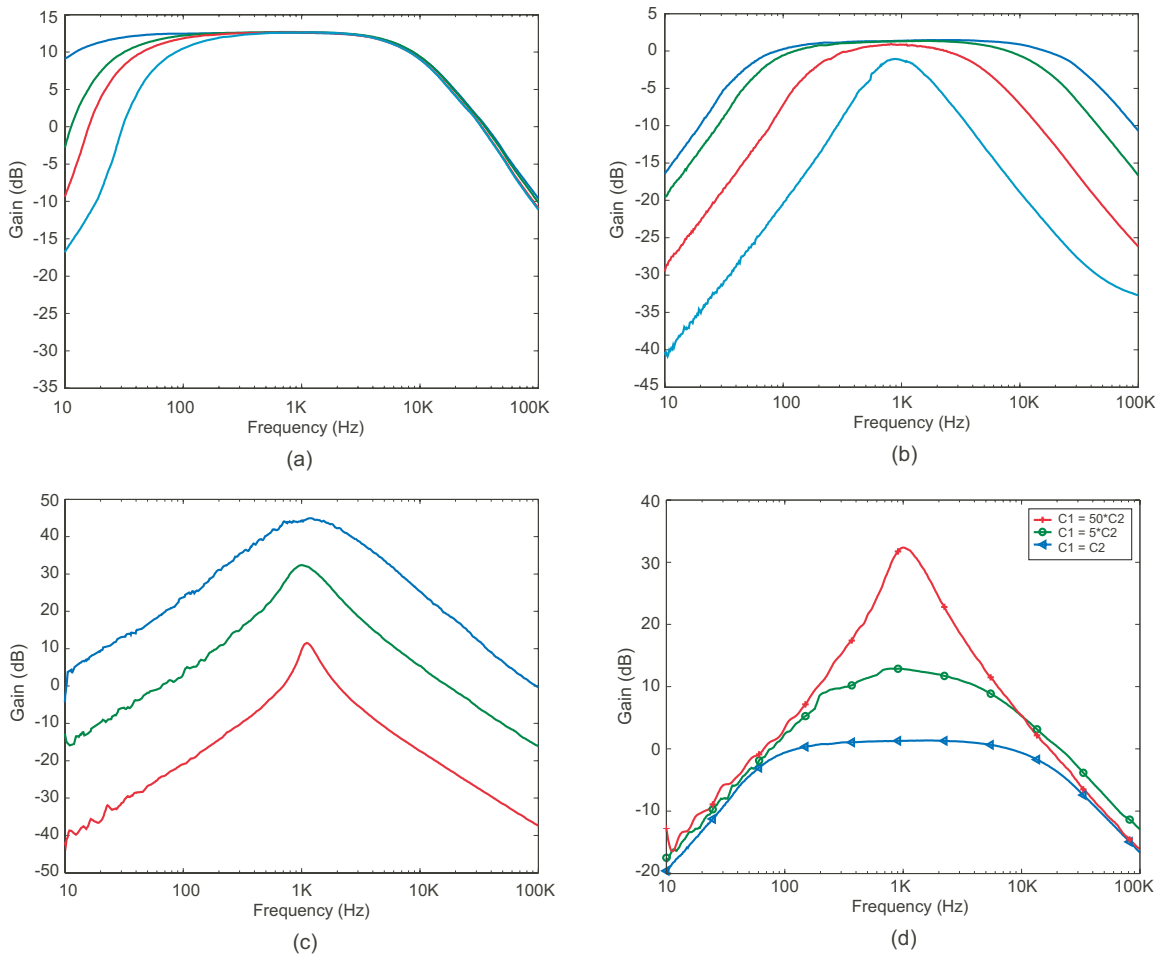

Fig. 2. C^4 frequency response curves. (a) Frequency response curve for a C^4 with a gain of 5. Showing that each corner frequency can move independently. (b) Unity gain C^4 showing tunability over a wide range of frequencies. (c) The Q for a C^4 can also be tuned, up to the maximum theoretical Q. (d) C^4 change in gain with C2. Data similar to earlier work [8].

side of the operating range. The plots of Fig. 2 show measured data from a $0.5\mu m$ process available through MOSIS that summarizes the frequency response of the C^4.

The C^4 takes on the properties of a bandpass filter with first-order roll-off and a pass-band gain set by the ratio of the two coupling capacitors as $A_v = -C_1/C_2$. The overlap capacitance of the MOSFET causes there to always be some effective C_2 capacitance, even if it is only a few fF, so the gain is not infinite. The overall time constant of the filter, which gives the center frequency, is

$$\tau = \sqrt{\tau_l \tau_h} \tag{2}$$

Furthermore, since the corner frequencies of the C^4 are completely independent of each other, as shown in Fig.2a, either one of the corner frequencies could be pulled to the extreme allowing the C^4 to take the form of a lowpass or highpass filter.

2. DESIGNING FOR Q

By tuning the filter such that $\tau_h > \tau_l$, resonance occurs, and the value of the Q peak is

$$Q = \sqrt{\frac{C_T C_O - C_2^2}{C_2^2}} \frac{x}{1 + x^2\left(\frac{C_O}{\kappa C_2} - 1\right)} \tag{3}$$

where

$$x = \sqrt{\frac{I_{\tau l}}{I_{\tau h}}} \tag{4}$$

Fig. 3 is a plot of the Q peak versus the ratio of I_{τ_l}/I_{τ_h} for a unity-gain C^4 using the extracted values of the capacitances from the layout. As can be seen from this MATLAB plot, there is a maximum value that the resonance can achieve. The maximum value occurs when I_{τ_h} is slightly larger than I_{τ_l} for the capacitances of the fabricated circuit that yielded

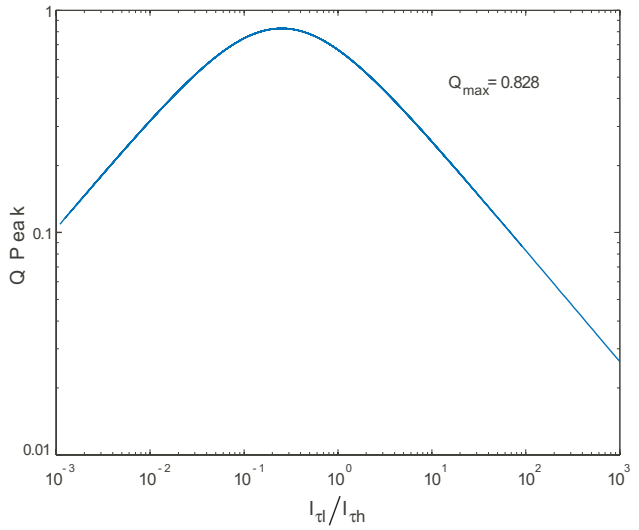

Fig. 3. Q as a function of I_{τ_h}/I_{τ_l}. There is a maximum Q at a particular current ratio, and the curve is relatively flat around that maximum point. The maximum achievable Q for this circuit was designed to be approximately 1. Higher maximum values of Q can be explicitly designed into the circuit.

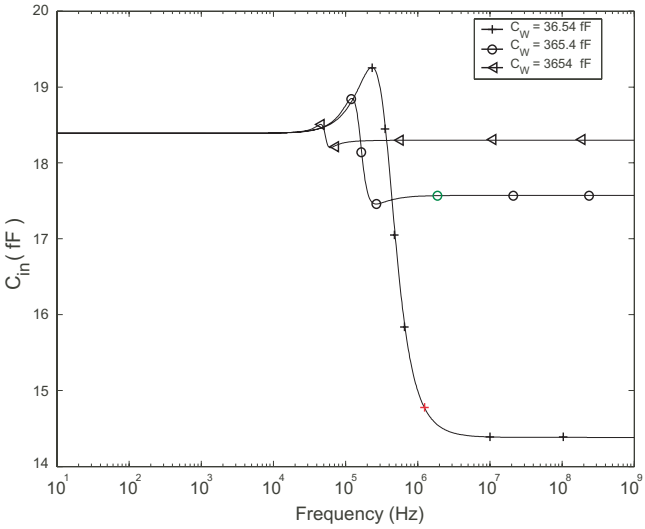

Fig. 4. Change in C^4 input capacitance vs. frequency. Low frequency input capacitance = C_1. This transitions to the high-frequency input capacitance which is roughly $C_1//C_w$.

the plots of Fig. 3. The maximum value of the Q peak can be predicted for a certain set of capacitances by taking the derivative of (3) and finding the maximum, and this is given by

$$Q_{max} = \frac{1}{2}\sqrt{\frac{\kappa\left(C_T C_O - C_2^2\right)}{C_2\left(C_O - \kappa C_2\right)}} \quad (5)$$

$$\approx \frac{1}{2}\sqrt{\frac{\kappa\left(C_1 + C_W\right)}{C_2}} \quad \text{for} \quad C_2 \ll C_O \quad (6)$$

This represents the maximum Q for small amplitudes and will drop as amplitude increases. This phenomena is not discussed within the scope of this paper, but will be discussed later. As can be seen from Fig. 3, the C^4 was not designed to have a large Q peak. However, by changing the capacitances, a much larger Q peak can be achieved. For example, by reducing the value of C_2, more resonance occurs. A good method to increase Q is to not explicitly draw any C_2 capacitance and use the gate-drain overlap capacitance of M4 in Fig. 1 as C2.

3. DESIGNING FOR MULTIPLE FILTER STAGES

One potentially hazardous trait of the C^4 is that the input capacitance of the circuit does not necessarily remain constant, but it varies based on frequency. This is particularly critical when cascading multiple C^4 stages to create higher order filter banks. If the previous stage in the overall system is dependant upon the input capacitance of the C^4 for its load capacitance, then this could be a serious issue.

Referring back to Fig. 1, the input capacitance can easily be found for the cases of very low frequencies and very high frequencies. For very low frequencies, the middle node is an AC ground because of the high-gain amplifier. Hence, the input capacitance for low frequencies is simply $C_{in} = C_1$. For very high frequencies, the transistors can no longer follow the signals, so the C^4 reduces to a network of capacitors and the input capacitance becomes the series/parallel combination of the capacitances in this network seen looking into the input, V_{in}. The input capacitance for the two extreme cases are given by

$$C_{in}(f \to 0) = C_1$$
$$C_{in}(f \to \text{inf}) = C_1 \| \left(C_W + C_2 \| C_L\right) \approx C_1 \| C_W \quad (7)$$

There is a transition region for the input capacitance between these states which occurs over a confined frequency band near the center frequency of the C^4. Fig. 4 shows results of a SPICE simulation in which the input capacitance was computed. Simulation and experiments closely agree for this circuit.

However, since the width of the swing in input capacitance is a function of the values of the capacitances, the effect of the input-capacitance shift can be minimized with a judicious choice of capacitor values. Increasing the drawn size of C_W is the best choice for reducing the shifting input capacitance for the simple reason that the larger the value of C_W, the more closely $C_1 \| C_W \approx C_1$, and hence the more closely the high-frequency C_{in} approaches the the low-frequency C_{in}. Fig. 4 shows the results of 10-fold increases in the capacitance of C_W. The larger that C_W is

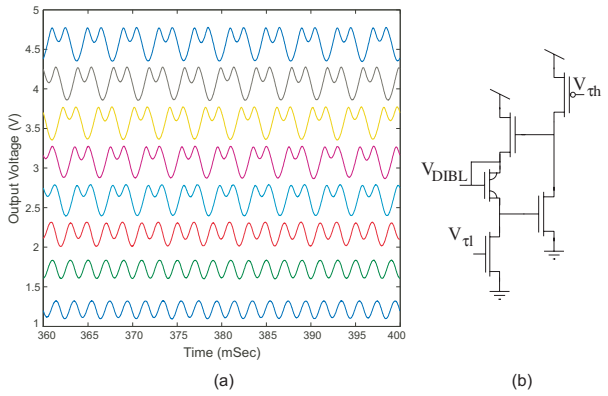

Fig. 5. (a) C^4 change in linearity with DIBL voltage. The linear range of a C^4 bandpass filter is improved by using source degeneration in the feedback path. A DIBL transistor is chosen to provide an exponential relationship that is more flat than a regular transistor because of it's very small early voltage. For simplicity each curve is offset +500mV. The lower curve shows the output when the DIBL voltage is closest to it's ideal voltage. (b) A circuit implementation to provide a self-bias for the DIBL transistor. The optimal DIBL voltage would be determined by the bias point of a given C^4, therefore a separate circuit would be required for each filter.

drawn, the less the effect of the input capacitance shift on the system.

Another way of reducing the effects of the shifting input capacitance is to put a buffer in front of the C^4 so that the previous circuit always sees the same load capacitance. However, for many cases, spending the real estate required for a buffer could be better used by simply increasing the size of the C_W capacitor because increasing C_W has advantages besides keeping C_{in} relatively fixed. The primary reason that C_W is drawn in the C^4 is to capacitively divide the input signal and thus increase the input linear range.

4. DECREASING DISTORTION

The C^4 uses a short-channel device, named a DIBL (Drain-Induced Barrier Loading) transistor, to decrease the loop-gain in the feedback path and increase the overall linearity of the device. A DIBL transistor is chosen to provide an exponential relationship that is more flat than a regular transistor because of it's very small early voltage. During initial characterization this device has it's gate pulled to VDD in order to remove it from the loop, however, an optimal bias point for the device is shown to improve linearity. Fig. 5(a) shows the decrease in the second harmonic as the DIBL bias approaches it's optimal value. The optimal DIBL voltage is dependent on the DC operating point, which changes with corner frequency for each filter. Fig. 5(b) shows a self-biasing scheme that is currently being testing to work over all frequencies thus increasing linearity without external biases. In the case of an array of these devices, the self-biasing DIBL circuitry would be required for each filter tap because V_{DIBL} is dependent upon $V_{\tau l}$ and $V_{\tau h}$, which change depending on the frequency response of the individual filter.

5. CONCLUSION

In this paper we have shown the design parameters which affect frequency response, gain and linearity of a 5 transistor filter element. We have shown primarily experimental results, along with some simulation, to verify the tunability and linearity of the device. Taking all of these into account, this ultimately results in a low-power and compact filter which can be easily tuned over 6 orders of magnitude in frequencies with maximum Q factors that can explicitly designed into a single stage. Using these design parameters, one can begin to design higher-order C^4 filter banks, with applications in numerous signal processing applications.

6. REFERENCES

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