A Regulated Charge Pump for Tunneling Floating-Gate Transistors

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***Abstract*— Flash memory is an important component in many embedded system-on-a-chip applications, which drives the need to generate high write/erase voltages in generic CMOS processes. In this paper, we present a regulated, high-voltage charge pump for erasing Flash memory and floating-gate transistors. This 0.069-mm^2 charge pump was fabricated in a 0.35 μm standard CMOS process. While operating from a 2.5 V supply, the charge pump generates regulated voltages up to 16 V with a PSRR of 52 dB and an output impedance of 6.8 kΩ. To reduce power consumption for use in battery-powered applications, this charge pump uses a variable-frequency regulation technique and a new circuit for minimizing short-circuit current in the clock-generation circuitry; the resulting charge pump is able to erase the charge on floating-gate transistors using only 1.45μJ.**

***Index Terms*— Analog memory, charge pumps, closed-loop systems, CMOS integrated circuits, flash memories, floating-gate transistors, short-circuit currents, tunneling, variable-frequency regulation.**

I. Introduction

THE most common form of solid-state nonvolatile memory is the floating-gate transistor—a CMOS-compatible device that is the basis of Flash memory [1] and that can also be used to create dense, low-power, programmable analog parameters [2]. Floating-gate transistors store information in the form of trapped charge on an electrically floating polysilicon gate. Under nominal operating voltages, this charge will remain fixed on the gate. To program a different amount of charge onto the gate, high voltages are used to induce Fowler-Nordheim tunneling and/or channel hot-electron injection, both of which enable electrons to pass through the gate oxide. Both tunneling and injection require voltages greater than the rated voltage of the core devices—even greater than the source/drain breakdown voltages in the case of tunneling—thus complicating the design of high-voltage generators in standard, single-well CMOS processes.

In this paper, we present a charge-pump topology fabricated in a standard 0.35μm CMOS process that is capable of providing the high voltages required for programming floating-gate transistors. We focus primarily on a charge pump for the tunneling operation since tunneling requires a high step-up ratio. Because the voltage across any single device in this charge pump never exceeds V_{dd}, this topology can easily be scaled for higher or lower output voltages, hence providing a means to produce the voltages required by other high-voltage on-chip applications, such as injection of floating-gate transistors or for MEMS devices. We also provide insight into the voltages that are required to generate tunneling conditions in floating-gate devices fabricated in standard CMOS processes as these processes scale to newer technology nodes.

Additionally, this charge pump has been designed for use in battery-powered applications in which power consumption must be minimized and the charge pump should be robust to noisy and/or drooping battery supplies. To meet these needs, we describe several circuit techniques, including: 1) a simple method for reducing start-up energy in a previously reported charge-transfer stage; 2) a method for regulating the charge pump via frequency modulation; and 3) a new circuit to minimize the short-circuit current of the clock circuitry. The topology we present can be easily designed to achieve a specific, and low, output ripple that is independent of the clock frequency and load current—low output ripple is crucial to precisely programming floating-gate transistors for applications in non-volatile analog memory and programmable analog biases. The resulting charge pump is able to provide a low-ripple output up to 16 V from a 2.5 V supply while expending only 1.45 μJ to erase floating-gate transistors.

We describe the development of this regulated charge pump in the remainder of this paper. Section II describes the voltage/current requirements for tunneling floating-gate transistors. Section III gives a brief overview of charge-pump fundamentals and then describes an unregulated, open-loop version of our charge pump. Section IV then presents a method of regulating charge pumps through frequency control, and Section V describes our current-controlled oscillator with a novel method for reducing short-circuit power consumption. Section VI describes the architecture of the complete regulated charge pump and presents measured results.

II. Considerations Regarding Tunneling Voltages and Scaling

Fowler-Nordheim tunneling is the process of moving electrons through an oxide using a large electric field [3]. This process is often used in floating-gate transistors to modify the charge stored on the floating gate and, accordingly, change the memory value. In many floating-gate applications

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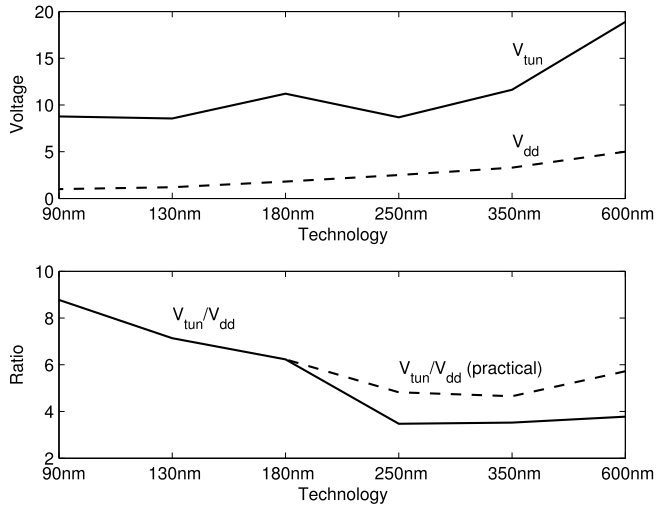

Fig. 1. Scaling of write/erase voltages in standard CMOS. (a) Scaling of critical programming voltages: the Fowler-Nordheim tunneling voltage (V_{tun}) and the core supply voltage (V_{dd}). (b) Ratio of the tunneling voltage to the core supply voltage.

in standard CMOS processes, tunneling is used for memory erasure [2], [4]. The tunneling current density can be approximated [5] by

$$J_{tun} \approx \alpha \exp\left(-\beta t_{ox}/V_{ox}\right) \tag{1}$$

where t_{ox} is the oxide thickness, V_{ox} is the voltage across the oxide, and $\alpha = 185.5\text{A}/\mu\text{m}^2$ and $\beta = 32.8\text{V/nm}$ are fits that we have extracted across multiple processes and device sizes [6].

As (1) illustrates, the Fowler-Nordheim tunneling current depends on the oxide thickness, which decreases with CMOS process scaling, resulting in lower tunneling voltages in smaller technology nodes. However, charge retention in floating-gate transistors is compromised by direct tunneling when $t_{ox} < 5\text{nm}$ [7], which gives rise to the continued use of 5–7 nm gate oxides in the newest NAND Flash processes while logic processes have continued scaling to a 2.5-nm physical gate oxide thickness [8], [9]. Consequently, floating gates that are built in standard processes below the 250-nm node should use thick-oxide I/O devices that are rated for operation at 2.5 V or greater so that oxide thicknesses are large enough to provide good charge retention.

Fig. 1(a) shows the scaling of floating-gate tunneling voltages in standard CMOS due to reducing the oxide thickness. The tunneling voltage (V_{tun}) was calculated for 1-ms erase times using (1) and typical trends in oxide-thickness scaling (e.g., [10], [11]). Noting that the voltage required for generating a tunneling current is much higher than the rated supply voltage for each process, a step-up voltage converter, such as a charge pump, must be used. A charge pump typically multiplies the chip V_{dd} by a certain value, which is expressed by the step-up ratio (V_{tun}/V_{dd}). The necessary step-up ratios to achieve tunneling in each technology node are shown in Fig. 1(b). The step-up ratio is lowest for the 250 nm through 600-nm nodes because: 1) below the 250-nm node, higher-voltage I/O devices are used to make low-leakage floating gates and 2) above the 600-nm node, devices are operated at 5 V even though they can accommodate much higher voltages. However, the rated V_{dd} of the 250-nm through 600-nm nodes produces noticeable hot-electron injection which can cause unwanted changes to the stored charge on a floating gate; consequently, these technology nodes must use lower supply voltages in practice, so the ratios for these nodes are essentially one integer value higher [see "V_{tun}/V_{dd} (practical)"].

In summary, Fig. 1 provides insight into the voltages that need to be generated by the charge pump for the tunneling voltage. Additionally, (1) provides constraints on the current output of this charge pump. The amount of load current required to tunnel a single floating-gate transistor is exponentially related to the inverse of the voltage across the tunneling oxide. Since the starting charge on the floating gate may be unknown and different for each tunneling operation, the current required to tunnel a device can vary greatly for each tunneling operation. Additionally, since tunneling is often used as a global erasure [4], many floating-gate transistors will likely be tunneled simultaneously by the same charge pump. With each floating-gate charge starting at different values, the load current of the charge pump cannot be known ahead of time and can vary by several orders of magnitude. Consequently, the charge pump providing the tunneling voltage must be able to provide a consistent voltage for a wide range of load currents.

Additional constraints on the charge pump that are specific to embedded analog applications include small size with minimal external components, reasonably fast start-up and shut-down, and consistent voltage generation in the presence of potentially noisy supply voltages; voltage consistency is especially important since it affects the programming accuracy. For generating tunneling voltages, which exceed the breakdown voltage of the devices, care must be taken in the design of the charge pump so that no individual device undergoes breakdown. Furthermore, for battery-powered applications, energy consumption should be minimized; therefore, the charge pump should only be enabled when it is needed to provide the high tunneling voltage. Finally, this charge-pump technology should be scalable to the tunneling-voltage requirements of other technology nodes. We demonstrate a charge pump in a standard $0.35\mu\text{m}$ CMOS process because of our existing applications of programmable and reconfigurable analog systems in this process [12], [13], and this same topology can be scaled to meet the needs of tunneling voltages in other processes, as well. In the remainder of this paper, we describe our design of an integrated high-voltage charge pump that is capable of meeting all these requirements.

III. Open-Loop Charge-Pump Architecture

A. Brief Overview of Charge Pumps

A charge pump, which is sometimes referred to as a voltage multiplier, is a switched-capacitor voltage converter that is often used to create voltages outside of the typical voltage rails (e.g., above V_{dd}). Fig. 2 shows an idealized Dickson charge pump [14], which is a standard charge-pump topology for integrated circuits because of its linear voltage growth and its insensitivity to stray bottom-plate capacitance. This charge

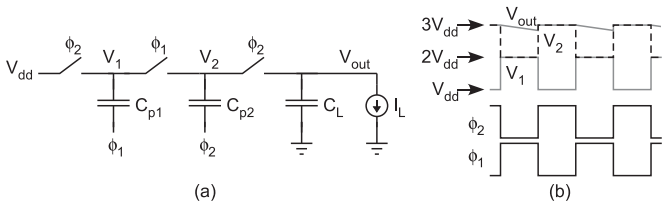

Fig. 2. (a) Ideal charge pump. (b) Operation of the ideal charge pump.

pump has two stages that are clocked by alternating clock phases (ϕ_1 and ϕ_2). When ϕ_1 is low (ϕ_2 is high), node V_1 and capacitor C_{p1} are charged to V_{dd}. On the subsequent clock phase, ϕ_1 transitions high, which raises the bottom terminal of C_{p1} to V_{dd}, thereby "pumping" V_1 to $2V_{dd}$; this resulting voltage at node V_1 is sampled at node V_2. When ϕ_2 goes high again, node V_2 is raised to $3V_{dd}$. The final output voltage is obtained by sampling the last stage onto the load capacitor, C_L. Higher voltages can be generated by cascading more stages, N. Each stage adds V_{dd} to obtain a total output voltage of $V_{out} = (N+1)V_{dd}$.

However, when a load current, I_L, is drawn from the charge pump, V_{out} is reduced. In equilibrium, the load draws a charge of $I_L T$ during each cycle of duration T which results in a voltage loss of $I_L T/C_p$ for each pumping capacitor. The resulting output voltage is

$$V_{out} = (N+1)V_{dd} - N\frac{I_L}{C_p f} \tag{2}$$

where $f = 1/T$ is the pumping frequency [15].

B. Charge-Transfer Switches

The primary challenge when designing a charge pump that approaches the ideal characteristics in (2) is the design of the charge-transfer switches (CTS), which are illustrated as ideal switches in Fig. 2. Early integrated charge pump designs used diodes or diode-connected transistors to implement the CTS [14]. Such designs rely upon the uni-directional current flow of diodes to only allow charge transfer onto a pumping capacitor when its voltage is exceeded by the voltage of the preceding stage. These designs suffer from poor voltage gain and poor efficiency because of the accumulation of diode voltage drops. As a result, several charge-pump circuits have been developed to dynamically control the on/off state of the CTS and, thus, improve performance.

As described in Section II, Fowler-Nordheim tunneling requires voltages so large that the drain-to-body junction will break down. To avoid break down, transistors in the CTS must inhabit isolated wells so that all voltage differentials in the CTS are at safe values. Since it is not always possible to isolate nFETs in standard CMOS processes, it is best for high-voltage charge pumps to use pFETs exclusively.

The all-pFET CTS that we use is based upon the circuits presented in [16], [17], and we have modified them to improve performance—particularly in reducing start-up power consumption. Our resulting charge-pump stage is shown in Fig. 3(b). Each stage has two parallel paths—a top path through M_{sw1} and M_{sw3}, and a bottom path through

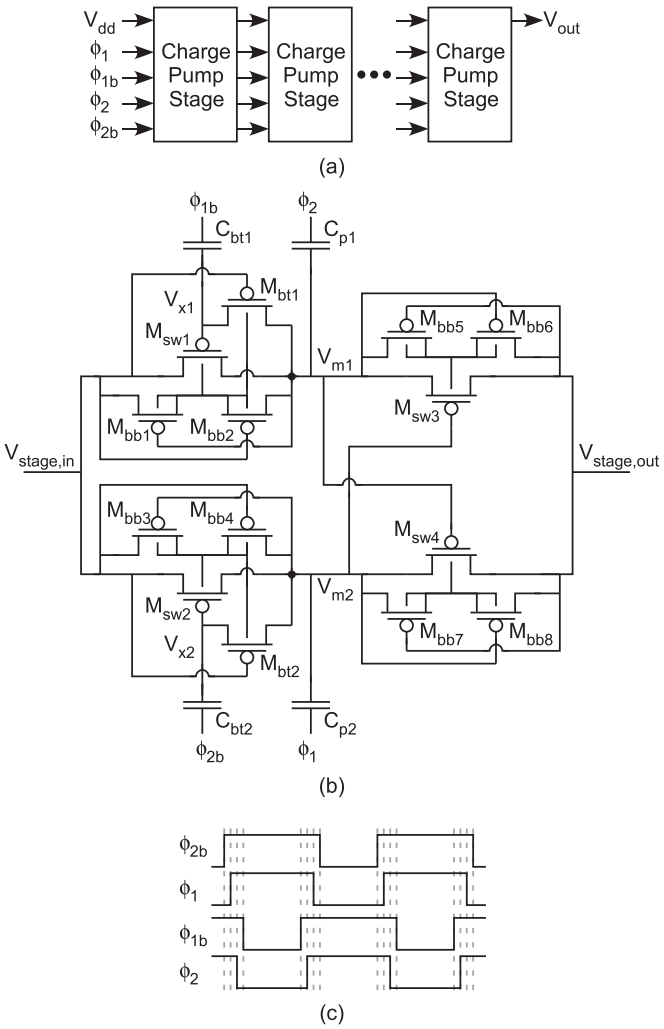

Fig. 3. (a) Open-loop charge pump consists of a cascade of charge-pump stages. (b) All-pFET charge pump stage that is used throughout this work. (c) Non-overlapping clock signals necessary for the charge pump stages.

M_{sw2} and M_{sw4}. The parallel paths conduct in opposite phases, which helps to reduce the output ripple. Furthermore, the opposing phases of the parallel paths offer a low-complexity means for clocking the second set of switches (M_{sw3} and M_{sw4}). This second set of switches reduces the voltage stress on the transistors in the off-phase. In a CTS with a single series switch, the voltage across an off switch is $2V_{dd}$. By adding the extra series switches, the off voltage is divided across the series switches so that no pair of terminals on the transistors is exposed to a voltage higher than V_{dd} [16], [17].

To provide the correct voltage for the transistor wells, the active well-biasing technique is used [18]. This technique is implemented by the "bulk-biasing" transistors M_{bb*}. Each pair of M_{bb*} transistors connects the well to the higher voltage terminal of the source or the drain. The system that was simulated in [17] extended the CTS of [16] by including active well biasing for switches M_{sw1} and M_{sw2} but not for M_{sw3} and M_{sw4}; instead, the wells of M_{sw3} and M_{sw4} were connected to $V_{stage,out}$. In steady state, this was acceptable because they included a grounded capacitor at $V_{stage,out}$ to hold the higher of V_{m1} and V_{m2}. However, we have removed

TABLE I
CHARGE PUMP SPECIFICATIONS

Technology	0.35μm CMOS
V_{dd}	2.5V
# Stages	6
C_{bt}	110fF
C_p	1.5pF
M_{bb}	3μm x 0.35μm
M_{bt}	3μm x 0.35μm
M_{sw}	5μm x 0.35μm

this capacitor and added well-biasing on these switches to avoid charging extra capacitance and activating parasitic vertical BJTs during startup, both of which unnecessarily consume power. Reducing the startup power is important for charge pumps that are used for tunneling floating-gate transistors; startup energy dominates the overall energy of the charge pump, particularly since the charge pump is turned on for relatively short periods of time while tunneling.

The operation of this charge-pump stage is as follows, where the phases of the 4-phase non-overlapping clock are depicted in Fig. 3(c). Focusing only on the top half of the circuit and noting that the bottom half is identical (and out of phase), we can see that charge is transferred from $V_{stage,in}$ to V_{m1} when M_{sw1} is turned on (ϕ_{1b} is low). When ϕ_2 goes high, node V_{m1} is increased by V_{dd}. This charge is then transferred to $V_{stage,out}$ when M_{sw3} is on (ϕ_1 is low). M_{bt1} is used to ensure that the correct voltage is on the gate of M_{sw1} at all times so that M_{sw1} is either fully on or fully off.

C. Complete Open-Loop Charge Pump

The complete, open-loop charge pump consists of six identical stages in series [Fig. 3(a) Top]. Although each charge-pump stage contains many devices, its size is dominated by the pumping capacitors C_{p*}. Each C_p is only half of the value needed for a charge pump with one capacitor per stage [15], so the size is similar to other charge pumps with commensurate performance. The design specifications are summarized in Table I.

Fig. 4(a) shows the output voltage of the six-stage open-loop charge pump for varying clock frequencies and load currents, and Fig. 4(b) shows the output resistance (which will be discussed in more detail in Section VI). As can be seen from Fig. 4(a), this charge pump is able to achieve the necessary voltages for tunneling a floating-gate transistor (approximately 10 V–12.5 V in this 0.35-μm CMOS process).

IV. REGULATION THROUGH FREQUENCY VARIATION

When a charge pump is used to generate tunneling voltages, V_{out} must be steady and consistent to facilitate accurate floating-gate programming. However, referring back to the idealized charge pump of Fig. 2, it is evident from (2) that V_{out} has an amplified dependence on the supply voltage, V_{dd}, which may be inconsistent and noisy in a battery-powered application. V_{out} also has a dependence on the load current I_L,

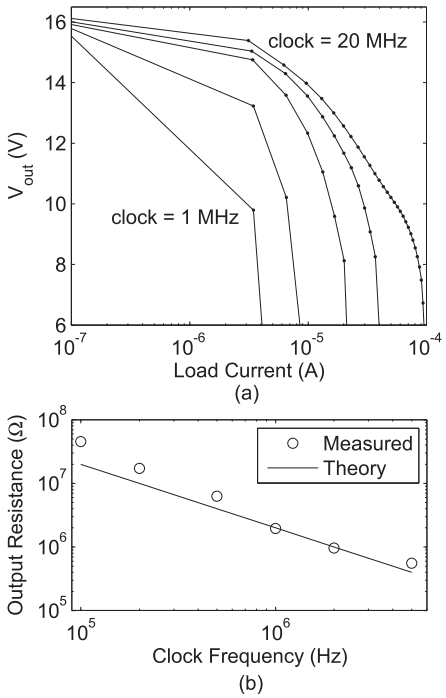

Fig. 4. Measured characteristics of the open-loop charge pump. (a) Output voltage characteristics as a function of load current for multiple clock frequencies $\in$ [1 MHz, 2 MHz, 5 MHz, 10 MHz, 20 MHz]. (b) Output impedance of our charge pump as a function of clock frequency.

which will vary as memory cells begin and finish programming; this dependence on the load current is clearly evident from the results of the open-loop charge pump [Fig. 4(a)] and can significantly vary the output voltage. Furthermore, in an open-loop charge pump, V_{out} is set to integer multiples of V_{dd}, which is a limitation for setting the sensitive program voltages to optimal values. To achieve reliable and accurate tunneling programming, the charge pump should be regulated to a constant output voltage.

Examining (2), only two quantities can be adjusted at runtime to regulate the output voltage: V_{dd} and f. Regulation using V_{dd} is typically accomplished by modulating the clocking voltages ϕ_1 and ϕ_2 [19], [20]. These clocking voltages contribute the NV_{dd} term of V_{out} in (2). These variable-pump-voltage regulators have the advantage of reducing the level of clock-feedthrough ripple on V_{out}, which must otherwise be removed with a large load capacitor. However, variable-pump-voltage regulators have the disadvantage that they constantly operate at their maximum frequency, which results in wasted power from unnecessarily charging and discharging all parasitic capacitances.

Variable-frequency regulators are thus a more efficient alternative. The simplest type of variable-frequency regulator is the "skip" regulator, which turns on a constant-frequency oscillator when V_{out} is less than the desired voltage and otherwise turns the oscillator off [21]. Some regulators have used a combination of variable-voltage and skip-mode [22], [23]. Skip regulators exhibit sporadic bursts of pumping which create large ripple on the output. A better alternative is a true "variable-frequency" regulator that linearly increases

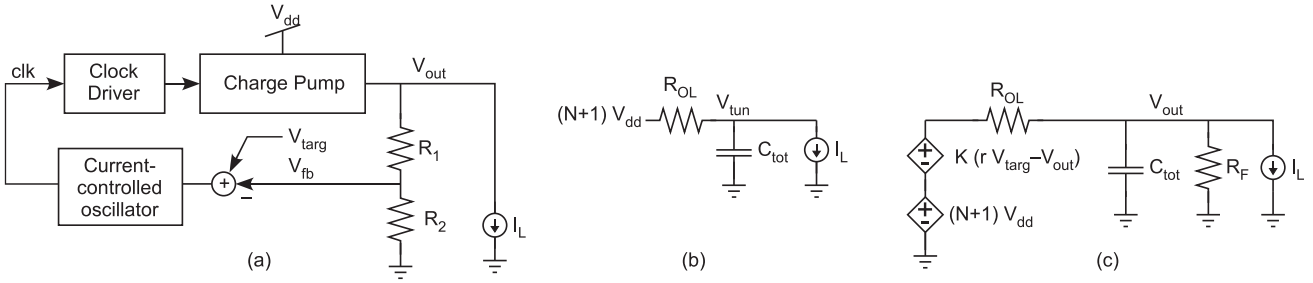

Fig. 5. (a) Block diagram of a regulated charge pump. (b) Linear model of an unregulated charge pump. (c) Small-signal model of a regulated charge pump.

TABLE II
CHARGE PUMP PERFORMANCE

	Open loop	Closed loop
Output resistance	$R_{OL} = N/(C_p f)$	$R_{CL} = R_{OL}/K$
Power supply rejection	$\text{PSRR}_{OL} = 1/(N+1)$	$\text{PSRR}_{CL} = K\text{PSRR}_{OL}$
Start-up time constant	$\tau_{OL} = R_{OL}C_{tot}$	$\tau_{CL} = \tau_{OL}/K$

TABLE III
CHARGE PUMP VARIABLES

N	Number of stages
V_{targ}	Target voltage
I_L	Load current
R_{OL}	Output resistance of open-loop charge pump
R_F	Resistance of voltage divider
$C_{tot} = C_L + C_{eq}$	Total output capacitance
C_L	Load capacitance
$C_{eq} = NC_p/3$	Distributed charge pump capacitance
$K = K_F K_{CP}/r$	Loop gain
K_F	Voltage-to-frequency gain of the error amplifier and oscillator
$K_{CP} = I_L N/(f^2 C_p)$	Frequency-to-voltage gain of the charge pump
r	Value of voltage division

or decreases the frequency to regulate V_{out}. This form of regulation has been previously used in [24], [25], and we have used the same basic method. In contrast to the voltage-doubler charge pump of [24] that used very-large external capacitors, we designed for small size and efficient operation at the high voltages/low load currents typical of tunneling. Furthermore, our charge pump achieves higher efficiency, smaller size, and better load regulation than the charge pump with a high step-up ratio in [25].

A generic block diagram for a variable-frequency regulated charge pump is shown in Fig. 5(a). A voltage-divider ($R_{1,2}$) reduces the output voltage to within the chip's rated voltage range. The difference between this reduced voltage and the desired voltage, V_{targ}, is used to modulate the pumping frequency until the output voltage locks onto the desired value. In addition to setting the output voltage, regulation also reduces the output resistance, increases the power-supply rejection, and decreases the start-up time compared to an open-loop charge pump.

The performance of an open-loop charge pump can be obtained by modeling it as the RC circuit shown in Fig. 5(b). From (2), the open-circuit voltage is $(N+1)V_{dd}$ and the open-loop output resistance is $R_{OL} = N/(C_p f)$. The total capacitance at the output, C_{tot}, combines the true load capacitance, C_L, with the distributed charge pump capacitance, $C_{eq} = NC_p/3$ [15]. The open-loop performance parameters are summarized in Table II.

It is more difficult to determine the closed-loop regulation performance because of R_{OL}'s dependence on the operating point (i.e., R_{OL} depends upon f, which is a function of V_{out} and I_L), which makes the regulation loop nonlinear. To simplify the analysis, the small-signal model from [25] is adapted and shown in Fig. 5(c). The variables are all defined in Table III. Sensitivity to V_{dd} has also been included in our model using the lower controlled voltage source of value $(N+1)V_{dd}$. The upper controlled source models the effect of the frequency-modulating feedback. The loop gain, K, is the product of: 1) the attenuation due to the voltage divider $(1/r)$; 2) the combined voltage-to-frequency conversion gain, K_F, of the error amplifier and oscillator; and 3) the frequency-to-voltage conversion gain of the charge pump

$$K_{CP} = \frac{dV_{out}}{df} = \frac{I_L N}{f^2 C_p}. \tag{3}$$

To solve for the regulation performance, first equate the currents at V_{out}

$$\frac{1}{R_{OL}}\left[(N+1)\,V_{dd} + K\left(rV_{targ} - V_{out}\right) - V_{out}\right] = V_{out}\left(sC_{tot} + \frac{1}{R_F}\right) + I_L \tag{4}$$

Then, solve for V_{out}, noting that by design $\frac{K}{R_{OL}} \gg \frac{1}{R_{OL}} + \frac{1}{R_F}$

$$V_{out} = \frac{rV_{targ} + \frac{N+1}{K}V_{dd} - \frac{R_{OL}}{K}I_L}{s\frac{C_{tot}R_{OL}}{K} + 1} = \frac{rV_{targ} + \frac{1}{\text{PSRR}_{CL}}V_{dd} - R_{CL}I_L}{s\tau_{CL} + 1}. \tag{5}$$

The output consists of a superposition of three components: the scaled-up target voltage, which is the desired output, as well as unwanted contributions from the supply voltage and the load current, which are both suppressed by the loop gain. The closed-loop performance parameters, which are summarized in Table II, are all improved by a factor of the

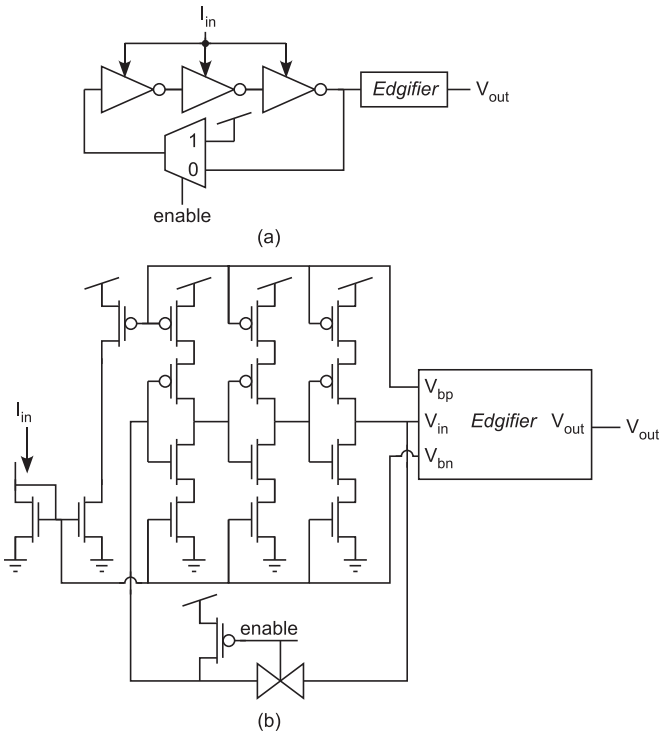

Fig. 6. Our three-stage current-controlled oscillator with low-power edge-sharpening. (a) Block diagram. (b) Schematic.

loop gain compared to the open-loop performance. It should be noted that the regulation circuitry adds little area and power compared to the rest of the charge pump. In Section VI, we will connect these performance parameters to actual circuit parameters.

V. Current-Controlled Oscillator and Edgifier

To modulate the frequency in our variable-frequency regulator, we have used a current-controlled oscillator. In comparison to voltage-controlled oscillators, current-controlled oscillators naturally offer linear input-to-frequency gain over a wide operating range, and are also easily limited so that the maximum frequency of the charge pump is not exceeded during transients. Our current-controlled oscillator, shown in Fig. 6, is based upon a three-stage current-starved ring oscillator. The frequency increases linearly with I_{in}. The current-to-frequency gain has been measured to be approximately 2 kHz/nA over a range of 100 Hz to 10 MHz.

A major attraction of variable-frequency regulation is that under light load conditions, the clock frequency reduces so that power consumption is minimized. However, the clock signals that are generated by low-frequency oscillators have long rise and fall times. These slow-moving edges create excessive short-circuit current when they are connected directly to a subsequent logic gate. Unlike the dynamic current that charges fan-out gates, this short-circuit current performs no useful function and should not be allowed to dominate the power consumption.

To minimize short-circuit power dissipation, we control the "push" and "pull" branches of an inverter with separate non-overlapping signals. This technique is most commonly used when driving large loads—such as in clock buffers [26] or in buck converters [27] —for which it is difficult to equalize the input and output rise/fall times, and for which the consequences of short-circuit current are dire because large transistors with large current-sourcing capabilities are used. Our contribution is to adapt this concept for use with slowly-varying input signals. We call this the "edgifier" concept because it transforms slow rise and fall times into sharp edges.

Our edgifier circuit, which is shown in Fig. 7(a), is based upon the CMOS buffer with non-overlapping gate drive presented by Yoo [26]. Yoo's circuit consists of a push/pull buffer ($M_{8T,B}$), the gates of which are driven by the logical AND of a) the input and b) the delayed and inverted version of the complementary gate signal. As a result, one transistor is always "turned off" before the other is "turned on." This technique reduces the short-circuit current of a buffer for which the load is not pre-determined [26]. However, the non-overlapping gate drive circuitry in [26] is still subject to short-circuit current from the slow rise and fall times of an input.

To minimize the short-circuit current that is caused by the slow rise and fall times of an input, we have added current-starving transistors $M_{3T,B}$ and $M_{7T,B}$ to the circuit's gate-drive front-end. The current-starving transistors limit the short-circuit current in the front-end, while allowing inverter $M_{8T,B}$ to be driven with non-overlapping signals. To enable transistors $M_{8T,B}$ to be strongly turned off, the current-starving transistors have only been used on one side of the logic ladder.

An additional benefit of asymmetric current starving is that it varies the trip point of the respective inverter. For example, the "top" inverters ($M_{1-7,T}$) have their trip points shifted toward higher voltages, and the "bottom" inverters ($M_{1-7,B}$) have their trip points shifted to lower voltages. The exact location of the trip point of the inverter can be tuned via the current-starving bias. For example, biasing $M_{3T,B}$ and $M_{7T,B}$ in the subthreshold domain significantly separates the "top" and "bottom" trip points while also limiting the switching current in those inverters.

As a result, our edgifier leverages the different trip points for the "top" and "bottom" paths caused by current starving to ensure that only one of $M_{8T,B}$ is turned on at any given time, as opposed to utilizing the delay properties of inverters as in [26]. The trip points of the "top" and "bottom" paths have been indicated in Fig. 7(b). The resulting operation of this circuit is analogous to a Schmitt trigger insofar as the output of the edgifier transitions from low-to-high at a different input voltage than it trips from high-to-low. However, the edgifier consumes significantly less power than a Schmitt trigger in this scenario of working with slow-transitioning clock signals.

Fig. 7 (b)–(e) compares simulation results between our edgifier and a CMOS inverter (which also consumes less power than a Schmitt trigger for this scenario) for an input signal with slow rise/fall times. In this example, the current-starving bias in the edgifier is a subthreshold current of 1nA and the outputs are unloaded. For the system-level implementation, this current-starving bias is derived as an "error signal" from a transconductor that measures the difference between the charge pump's desired and actual output voltage. The

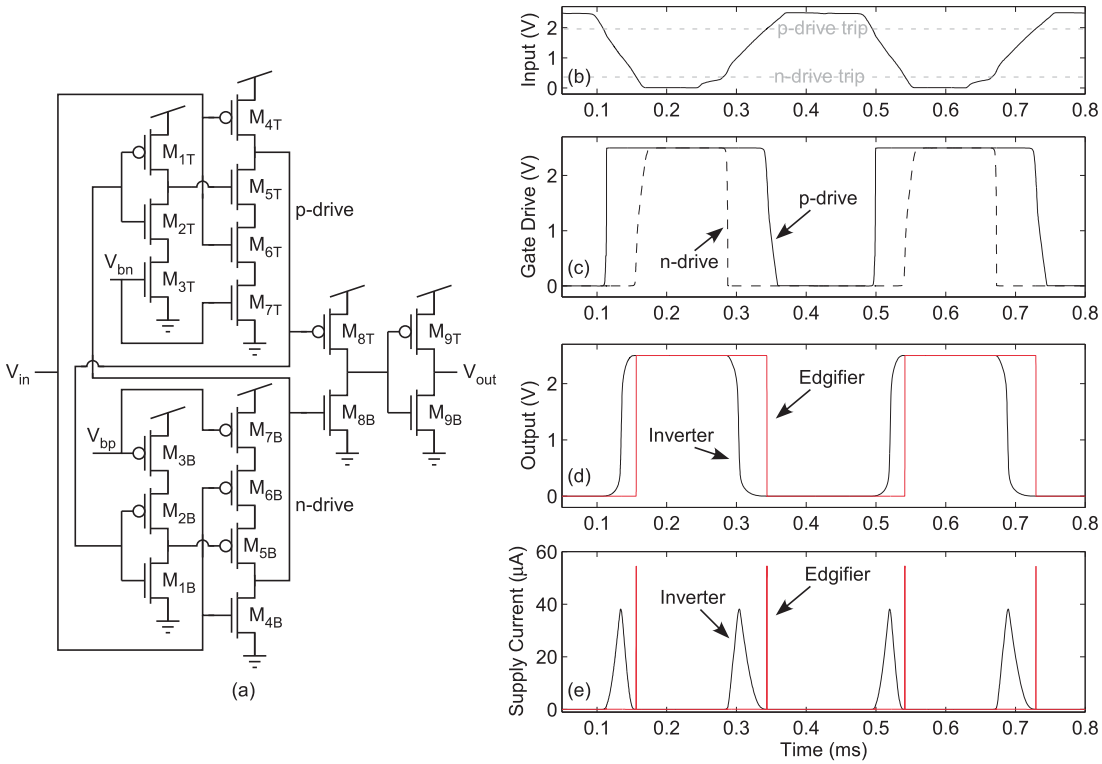

Fig. 7. (a) Our "edgifier" circuit drives inverter $M_{8B,T}$ with non-overlapping gate signals to minimize the short-circuit current that would otherwise result from slowly rising/falling input signals. (b)–(e) Simulation results comparing the edgifier to a single inverter. (b) Input generated by ring oscillator. (c) Non-overlapping gate drive signals generated by the edgifier. (d) Output signals of an edgifier and an inverter in response to the slowly rising/falling input in (b). (e) Supply current of an edgifier and an inverter. Non-overlapping gate drive significantly reduces the energy of each edgifier transition.

simulated output of the ring oscillator is used as a realistic input to the circuits [Fig. 7(b)]. The output of the edgifier is shown in Fig. 7(d), and is compared to the output of an inverter in response to the same input. This inverter has the same dimensions as $M_{9T,B}$. Fig. 7(e) shows that the inverter draws supply current over a long duration on each transition. In comparison, the edgifier's supply current is only a short impulse.

The edgifier's reduction in the short-circuit current of subsequent logic gates can significantly reduce the overall power consumption of a circuit that contains a low frequency oscillator. This power reduction is shown in Fig. 8. Measured and simulated power consumption values are shown over a wide range of frequencies. The power consumption "w/ edgifier" includes the oscillator, edgifier, and one subsequent logic gate. The power consumption "w/o edgifier" includes the oscillator and one subsequent logic gate. Because of the current-starved delay elements in the oscillator, the rise and fall times of the oscillator are a constant percentage of the clock period, which results in constant short-circuit power consumption for the logic gate "w/o edgifier" below 1MHz. In contrast, the power consumption of the oscillator "w/ edgifier" continues to reduce by almost three decades, enabling the total power of the charge pump to reduce further at low load currents.

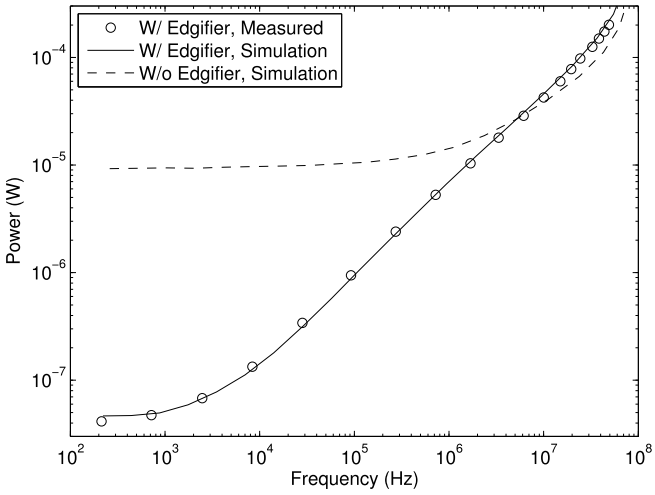

Fig. 8. Power versus frequency of our current-controlled oscillator. The placement of an edgifier prior to any digital logic allows the power to reduce with frequency over a much larger range. The supply voltage is 2.5 V, and the current-starving bias for the edgifier scales with the current-starving bias of the clock generator circuit.

VI. The Complete Charge Pump

Fig. 9(a) shows the schematic of our complete regulated charge pump. This charge pump was fabricated in a standard n-well 0.35μm CMOS process, and the die photograph of the 230μm $\times$ 300μm charge pump is shown in Fig. 10. Instead of using linear resistors in the voltage divider, we used eight diode-connected pFETs, each in their own well, to reduce the overall size [Fig. 9(b)]. Fig. 9(d) shows measurements of the current draw of the divider branch at different voltages. The divider branch was designed to draw 100 nA–1 μA over the typical operating range (V_{out} = 10 V–12.5 V), which

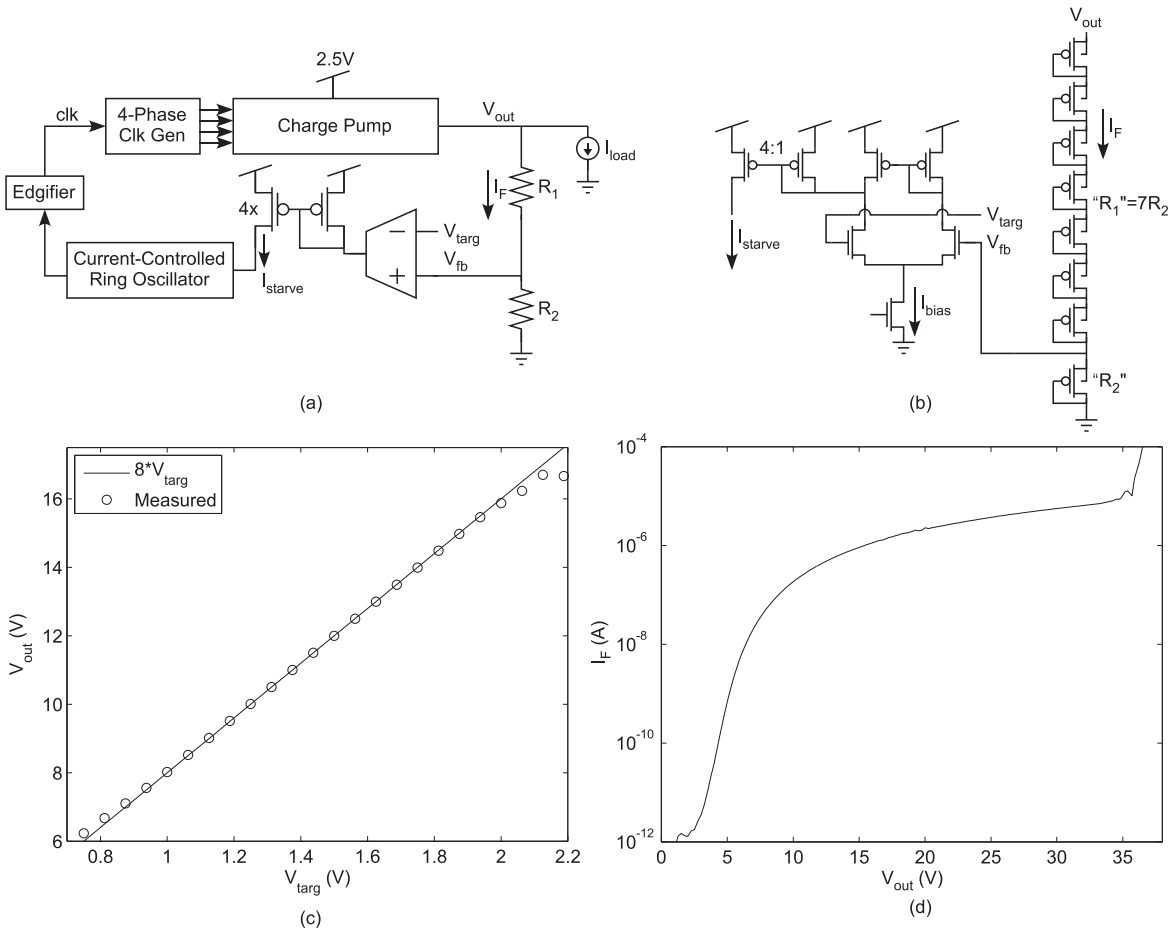

Fig. 9. (a) Block diagram of our complete regulated charge pump. (b) Transistor-level details of the OTA and the diode-connected transistors used to implement the "resistive" divider in (a). (c) Measured dc-dependence of the charge-pump output on V_{targ} for a purely capacitive load. (d) Measured current–voltage sweep of the pFET-divider circuit. The well-to-substrate breakdown current can be seen in the top-right. This breakdown is not a concern because it occurs at a much higher voltage than the circuit's operating voltage. This result also indicates that well-to-substrate breakdown voltage is not an issue for the operating range of voltages for this charge pump.

Fig. 10. Die photograph of the complete regulated charge pump circuit. The size is 230μm $\times$ 300μm.

is a sufficient minimum load current to prevent the clock frequency from dropping below 10 kHz. This minimum clock frequency maintains stable regulation when the target load is primarily capacitive (e.g., an array of tunneling junctions) without unnecessarily wasting power.

By dividing V_{out} by a factor of eight in Fig. 9(a), V_{out} is thus regulated to $8V_{targ}$. The measured transfer curve from V_{targ} to V_{out} is shown in Fig. 9(c). From 7.5 V to 16 V, the average steady-state output voltage is regulated to within 1% of $8V_{targ}$ (with a small ripple voltage, which will be discussed shortly). Deviation at the high voltages is caused by the open-loop charge pump's maximum voltage $(N+1)V_{dd} = 17.5V$. In Fig. 9(a), error amplification is achieved by using an operational transconductance amplifier (OTA) to convert the error into a current, as opposed to using the voltage output of an operational amplifier or comparator which is typically used in "skip" regulators. Deviation at the low voltages in Fig. 9(c) is caused by the error-amplification OTA's bias transistor being pushed out of the saturation region.

Now that the complete details of the regulated charge pump have been elaborated, we can calculate the loop gain K that was described in Section IV. Starting from V_{out}: V_{out} is divided by $r = 8$, then it is converted to a current with transconductance G_m, a current mirror scales this current by a factor of 4, the current-controlled oscillator then converts this current to a frequency with a gain of $K_{RO} = 2$ kHz/nA, and finally, the charge pump converts this frequency to the output voltage with a gain of K_{CP}. The total loop gain is the product of all of these components

$$K = \frac{4G_m K_{RO} K_{CP}}{r} \tag{6}$$

The transconductance provides a way to tune the charge pump for the desired loop gain, which changes the load-regulation characteristics and the start-up time. Using (2), the dependence of the clock frequency on the load current is given by

$$f = \frac{NI_L}{C_p\left[(N+1)V_{dd} - V_{out}\right]} \tag{7}$$

where C_p is the pumping capacitance per stage. By combining (3), (6), and (7), the loop gain can be expressed as

$$K = \frac{4C_pG_mK_{RO}}{rNI_L}\left((N+1)V_{dd} - V_{out}\right)^2. \tag{8}$$

In addition to dependence upon G_m, the loop gain is also dependent upon I_L and the desired V_{out}. Of note, the loop gain increases with decreasing I_L; however, the loop gain remains finite due to the effective load current through the resistive divider in the feedback loop, thereby keeping the system stable for capacitive loads. While loop gain decreases with increasing V_{out}, it maintains a value >100 even for an output of with a purely capacitive load. Performance with capacitive loads and small I_L is an important consideration when tunneling floating-gate transistors; this charge pump is able to set $V_{out} = 8V_{targ}$ to within 1%, as was shown in Fig. 9(c).

Using K and (2), we can obtain the closed-loop output resistance from Table II

$$R_{CL} = \frac{R_{OL}}{K} = \frac{r}{4C_pG_mK_{RO}}\frac{N}{(N+1)V_{dd} - V_{out}}. \tag{9}$$

To verify this expression, we have measured the open-loop and closed-loop load regulation in Figs. 4(a) and 11(a). The improvement afforded by regulation is clearly evident. Indeed, it would be very difficult to precisely generate an arbitrary high voltage without regulation. The output impedance is extracted from these data and is shown in Figs. 4(b) and 11(b). Good agreement is found between the measured results and the theoretical values for R_{OL} and R_{CL}. This agreement confirms that, when the charge pump is designed to sufficiently approach ideal characteristics, this simple analysis can be used to confidently design a high-voltage charge pump.

Additionally, (9) helps provide insights into the stability of this system. Since R_{CL} has no dependence on the load current, the corner frequency of this system only depends on G_m (which is generally set to a fixed value) and the desired V_{out}. Decreasing V_{out} increases the bandwidth of the system by modifying the output pole, which is the dominant pole of the charge pump. For V_{out} within typical values for generating tunneling voltages (e.g., $>$ 7.5V), all non-dominant poles are at sufficiently high frequencies so as to not cause any stability issues, whatsoever. For values of $V_{out} < 7.5$V where instability could become an issue, stability can be maintained with this topology by increasing C_L to keep the dominant pole sufficiently low, or by reducing the number of stages.

In a circuit that operates beyond the rated voltage of the process, the designer should ensure that the local voltage differentials for each device are within the rated voltage range. A beneficial feature of the charge pump stage [Fig. 3(b)] is that the use of two series switches in each stage protects the devices from any voltage stress greater than V_{dd} [17]. To verify that this protection ensures reliable performance under typical operating conditions, we measured the charge pump's output resistance before and after the charge pump had generated 10^6 12.5V-pulses of 1ms duration. These pulses are typical of the way the charge pump is used to program floating-gate transistors. The before-and-after measured output resistance is shown in Fig. 11(b). The "burned in" charge pump consistently has a slightly higher output resistance. However, the variation is small, and the number of cycles is greater than the typical rating for Flash memory, which confirms that this charge pump has sufficient long-term reliability for our application.

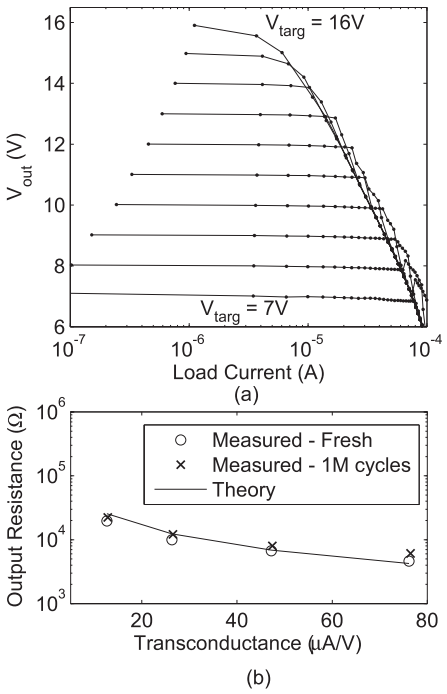

Fig. 11. (a) Measured load regulation characteristics of the closed-loop charge pump. V_{targ} was varied from 7 V to 16 V in increments of 1V. (b) Measured DC output impedance of our charge pump as a function of G_m (which was varied by modifying the bias current of the OTA). To validate reliability, the measurement was performed with a fresh charge pump, as well with a charge pump that had previously generated 10^6 12.5V-pulses.

The prominent characteristic of a frequency-regulated charge pump is that the frequency varies, which helps to minimize the power consumption once the target output voltage is reached. Fig. 12 shows a measurement of the charge pump generating a 1-ms, 12.5-V tunneling pulse. The measured frequency of the clock over time is shown in Fig. 12(c). During startup, the OTA is saturated and the clock pumps at a maximum frequency of $\sim$ 30 MHz. Once the target voltage is reached, the clock is relaxed to $\sim$ 300 kHz. The resulting mitigation in supply current while the voltage is held is seen in Fig. 12(b) which is especially pronounced because the clock frequency is slow enough that the edgifier produces additional power savings (see Fig. 8). The overall energy that was used to generate this pulse was 1.45μJ.

Fig. 12(a) also shows the output voltage ripple, ΔV, for the charge pump in steady-state. The standard expression for output ripple in charge pumps is given by

$$\Delta V = \frac{I_L \Delta t}{C_L} \tag{10}$$

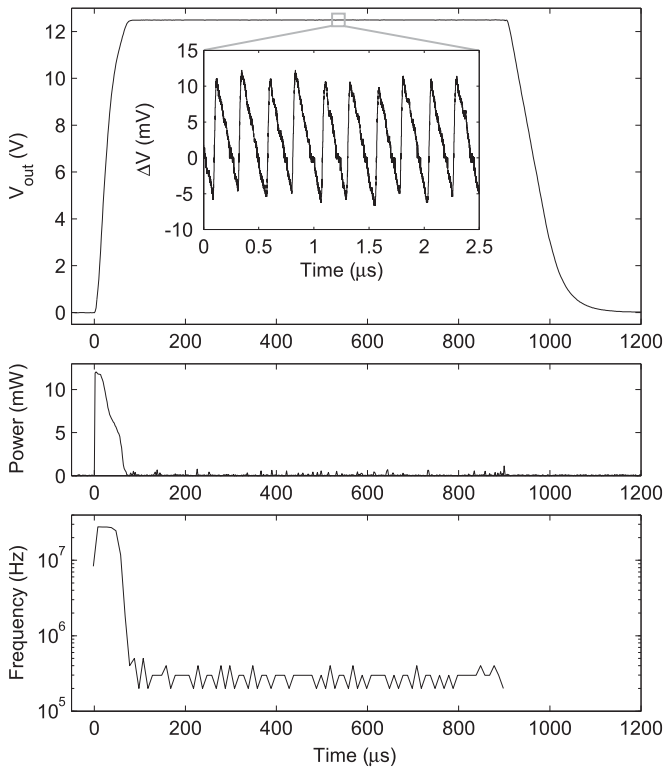

Fig. 12. Measured transient characteristics of our closed-loop charge pump. (Top) Output voltage with an inset of the ripple voltage, ΔV. (Middle) Instantaneous power consumption. (Bottom) Closed-loop adapted clock frequency.

where C_L is the capacitance loading the output node, I_L is the load current that discharges C_L, and Δt is the period of the ripple which is established by the clock frequency; for our charge pump that uses a parallel structure, Δt is half the clock period (i.e., twice the clock frequency). Since our charge pump leverages variable-frequency regulation, the frequency of the clock depends on I_L as given by (7). Therefore, the total output ripple voltage for our charge pump is

$$\Delta V = \frac{C_p}{2NC_L}\left[(N+1)\,V_{dd} - V_{out}\right]. \tag{11}$$

Of note, the ripple voltage of our charge pump has no dependence on the load current or the clock frequency, whereas a charge pump that does not employ variable-frequency regulation has these dependencies [see (10)]. Instead, the ripple voltage can be designed to have a specific value by setting appropriate values for the pumping capacitance and the load capacitance. Our charge pump had a measured ripple of $< 18\ mV$ when driving a load capacitiance of approximately $80pF$, which was created primarily from parasitic capacitances from the pads, board-level connections, and oscilloscope probes (i.e., no explicit load capacitor was used).

The efficiency of a charge pump is the power delivered at the output of the charge pump divided by the total power going into the circuit, given by

$$\gamma = \frac{V_{out} I_L}{V_{dd} I_{vdd}}. \tag{12}$$

For our regulated charge pump, this input power includes the power consumed by all components, not just the charge pump. We have not emphasized efficiency because it is not a crucial specification when generating short tunneling pulses for tunneling junctions that draw a very small load current. As can be seen in Fig. 12, most of the energy is consumed while starting up the charge pump. However, we will briefly discuss efficiency because it is a standard comparison point for voltage converters and because it will be of interest for modifying this charge pump for other applications, such as for injection-level supply voltages for floating-gate programming and also for various MEMS applications.

From [15], the supply current of an ideal charge pump with bottom-plate stray capacitance is

$$I_{vdd} = \left[(N+1) + \alpha\frac{N^2}{(N+1)V_{dd} - V_{out}}V_{dd}\right] I_L \tag{13}$$

where α is the ratio of the bottom-plate stray capacitance to the pumping capacitance, which is fixed for a given CMOS process and is typically in the range of 0.1–0.2. The first additive term accounts for the current that is pumped toward the load. The second term accounts for the current that charges and discharges the stray capacitance. The theoretical maximum efficiency is

$$\gamma = \frac{V_{out}}{V_{dd}\left[(N+1) + \alpha\frac{N^2}{(N+1)V_{dd} - V_{out}}V_{dd}\right]}. \tag{14}$$

For $V_{out} = 12$V, $N = 6$, and $V_{dd} = 2.5$V, the maximum theoretical efficiency is approximately 52%. Fig. 13(a) shows the measured efficiency of the open-loop and closed-loop charge pump for varying load currents. Fig. 13(b) also shows how the efficiency changes according to the step-up factor (for multiple values of I_L). The charge pump achieves approximately 65% of the theoretical efficiency. Furthermore, the overhead of regulation has not significantly decreased the efficiency of the unregulated charge pump. In fact, variable-frequency regulation is able to achieve better regulation across a wider range of load currents.

Since the charge pump was designed for use in ultra-low-power systems where the supply voltage is provided by batteries or energy harvesting and may vary significantly over time, power-supply rejection is an important concern. The use of regulation improves the power-supply rejection by 68dB over an open-loop charge pump. The measured power-supply rejection ratio (PSRR) for the regulated charge pump was 52 dB at 1 kHz with $V_{out} = 12$V.

Table IV compares our charge pump to others—specifically, we compare our charge pump to other regulated charge pumps that have been fabricated and are capable of producing voltages that are twice the rated voltage of the core devices (i.e., $V_{out} > 2V_{dd}$). The last row of this Table indicates whether or not the particular charge pump can achieve large-enough voltages for tunneling floating-gate transistors in their respective process. Even though a constant and predictable charge-pump output voltage is critical for many memory applications (e.g., multi-level Flash [33] and analog non-volatile memory [2]), very few regulated high-voltage charge pumps have been reported. As can be seen from this table, our charge pump is able to provide good performance while

TABLE IV
COMPARISON OF REGULATED HIGH-VOLTAGE CHARGE PUMPS

	This Work	Aaltonen [25]	Barnett [28]	Kang [21]	Kim [29]	Tsai [30]	Tsai [31]	Tseng [32]
Process	0.35μm	0.35μm HV	0.35μm	63nm	0.13μm	0.18μm	0.18μm	0.18μm
V_{in} (V)	2.5	2.5	2–3	1.8	1.2	1.8	1	1.2
V_{out} (V)	7.5–16	10	13.2–14.1	1–18	3	$\pm$6	3–6	6
Max Step-Up	6.4	4	7.05	10	2.5	3.33	6	5
N	6	9	8	45	3	3	6 stages by 9 interleaved cells	3
Effective Step-Up per Stage	1.07	0.44	0.88	0.22	0.83	1.11	1	1.67
Total C_{pump} (pF)	18	14.4	–	225	240	–	–	–
Size (mm^2)	0.069	0.14	0.092	>2.56	0.6	4.94	0.5	4
Efficiency	34% @ 25μA	18% @ 29μA	–	–	12.5% @2mA	–	48–58% 52% @ 240μA	–
Maximum Load Current	40μA @10V	–	<5μA	150μA	2mA	400μA	240μA	700μA
Ripple (mV)	18	–	–	200	–	–	39	30
Tunneling Possible?	Yes	Yes	Yes	Yes	No	No	No	No

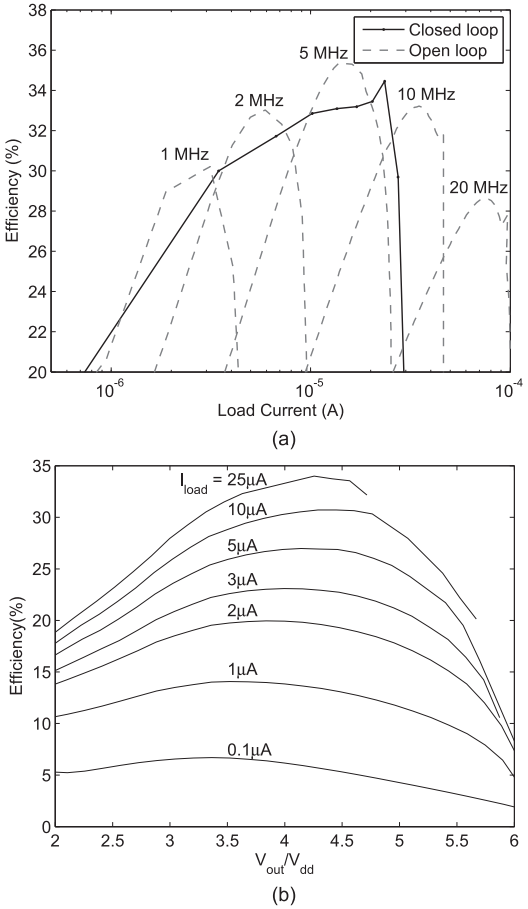

Fig. 13. Measured efficiency of the charge pump. (a) Measured open-loop and closed-loop efficiency for varying load currents. The closed-loop charge pump was measured with $V_{out} = 12$V. (b) Measured efficiency for varying step-up factors and multiple load-current conditions.

maintaining a small size. Additionally, our charge pump is able to provide a high voltage with very little ripple, and (11) describes how this ripple can be improved even further.

VII. CONCLUSION

In this paper, we have presented the design and results of a regulated high-voltage charge pump for generating tunneling voltages to program floating-gate transistors. This compact charge pump leverages variable-frequency regulation and a new circuit for minimizing short-circuit current to provide reliable tunneling voltages while consuming very little power. Because of its compact size and low-power operation, this charge pump is ideally suited to battery-powered applications. Additionally, it can easily be adapted to provide higher or lower voltages for programming floating-gate transistors in scaling CMOS processes and also for other applications, such as MEMS devices.

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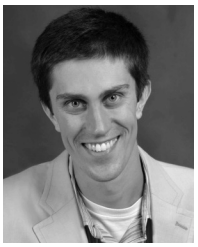

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