Demo Abstract: Hibernets: Energy-Efficient Sensor Networks Using Analog Signal Processing

Brandon Rumberg David W. Graham Vinod Kulathumani
Lane Department of Computer Science and Electrical Engineering
West Virginia University
brumberg@mix.wvu.edu, {david.graham, vinod.kulathumani}@mail.wvu.edu

ABSTRACT

In-network processing is recommended for many sensor network applications to reduce communication and improve energy efficiency. However, constraints on memory, speed, and energy currently limit the processing capabilities within a sensor network. By integrating ultra-low-power analog circuitry with sensor nodes, we can reduce the node's power consumption and extend the node's processing capacity. We present a custom analog front-end which performs spectral analysis at a fraction of the power used by a digital counterpart. This front-end has been combined with a TelosB mote to (1) selectively wake up the mote based upon spectral content of the signal, thus increasing battery life without missing interesting events, and to (2) achieve low-power signal analysis using an analog spectral decomposition block, freeing up digital computation resources for higher-level analysis.

Categories and Subject Descriptors

B.7 [**Integrated Circuits**]: Miscellaneous;
C.3 [**Special-purpose and Application-Based Systems**]: Real-time and embedded systems, Signal processing systems; B.8 [**Performance and Reliability**]: Miscellaneous

General Terms

Design, Performance, Measurement

Keywords

Analog Signal Processing, Energy-Efficient, Selective Wake Up, In-Network Processing, Sensor Networks

IPSN'10, April 12–16, 2010, Stockholm, Sweden.
ACM 978-1-60558-988-6/10/04.

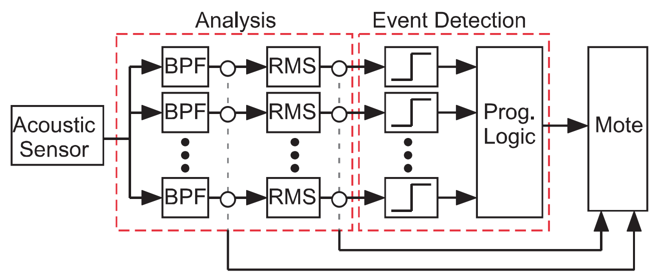

Figure 1: Augmenting a sensor node with an analog signal processor (ASP). The signal analyzer extracts features, in this case spectral features, for the event detector and performs pre-processing which would otherwise need to be performed by the mote. The event detector performs selective event detection, allowing the mote to sleep without dropping events.

1. INTRODUCTION

Wireless sensor networks (WSN) are promising for applications such as vibration monitoring and acoustic object classification [1, 4, 2, 6]. These applications require the nodes to sense frequencies up to 100kHz. Such frequencies require local processing to reduce communication overhead. The amount of signal processing demanded is difficult to obtain with the strict energy budgets that are required for a mote to last for long durations on small power sources, such as batteries and energy harvesting systems. These factors prevent the wide-scale deployment of sensor networks for applications of even moderate signal frequencies. This demonstration exhibits the findings in [5].

2. HIBERNETS DESIGN

We propose augmenting sensor nodes with ultra-low-power analog signal processing (ASP). ASP systems [3] can extend the capabilities of the mote while contributing little to the node's required power budget. We suggest an ASP/WSN framework (Figure 1), in which the

ASP consists of two parts: signal analysis and event detection / classification. The analysis portion serves dual purposes: (1) generate features for use in event detection and (2) perform pre-processing to free up the mote's computing resources. The classifier wakes the mote when it detects events of interest, and allows the mote to operate at a higher abstraction level, dealing with sensor data at the level of classes.

To demonstrate the potential of the ASP/WSN framework, we have designed and fabricated an analog integrated circuit for use in wireless sensor networks. The analysis portion of the system performs spectral decomposition using a constant relative-bandwidth filter bank with subband root-mean-square (RMS) detectors. Event detection is performed with a comparator on the RMS output of each subband, followed by digital logic which asserts a hardware interrupt when the signal spectrum matches a user-defined binary template. The core of this chip operates at an average power of $1 - 3\mu W$, which is less than the power consumed by a TelosB mote in its lowest-power sleep mode.

3. DEMONSTRATION

We demonstrate the incorporation of a custom analog integrated circuit with a sensor node, and highlight (1) low-power event detection and (2) pre-digitized signal analysis. In order to show the impact that analog signal processing can have on wireless sensor networks, we exhibit two motes, one with ASP and the other without ASP. Each mote is equipped with a low-power acoustic sensor, and we compare each mote's power consumption and CPU utilization in an acoustic event detection scenario. Our system detects events based on spectral content (i.e. presence of signal in a particular combination of frequency bands). Upon detecting an event, the mote transmits the spectral analysis output to the basestation for visualization (similar to Figure 2). We will demonstrate the ability to use the mote to adjust both the ASP settings and the event detection rules. A laptop running sound synthesis software will allow users to create acoustic events, and evaluate each mote system's ability to distinguish between sounds in a noisy environment.

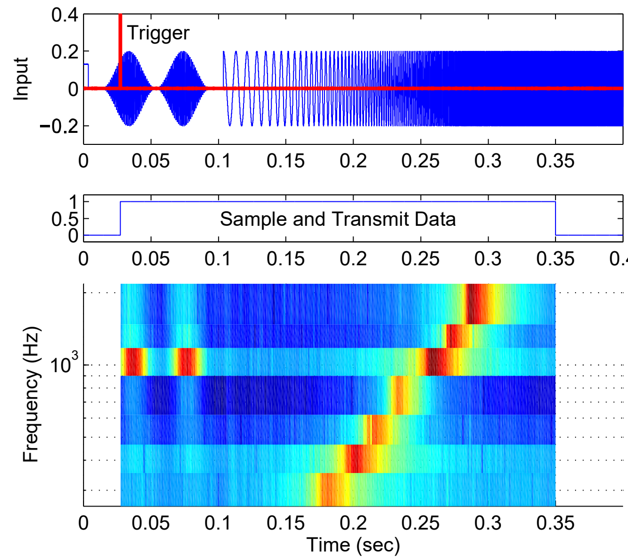

Figure 2: Spectral analysis performed by the analog IC. The spectral decomposition representation (RMS output of all frequency bands) is sampled by the mote and then transmitted to the base station. (Top) The input signal is composed of two 1kHz pulses followed by a logarithmic chirp signal. The 1kHz band comparator output serves as a trigger to begin sampling all eight channels. (Middle) Once the trigger goes high, the ADC samples all 8 channels for a user-specified amount of time. (Bottom) Spectrogram of the frequency-dependent magnitude data received by the base station.

4. REFERENCES

[1] A. Arora, P. Dutta, S. Bapat, V. Kulathumani, H. Zhang, and V. N. et. al. A Line in the Sand: A Wireless Sensor Network for Target Detection, Classification, and Tracking. *Computer Networks, Special Issue on Military Communications Systems and Technologies*, 46(5):605–634, July 2004.

[2] M. Duarte and Y.-H. Hu. Vehicle classification in distributed sensor networks. *Journal of Parallel and Distributed Computing*, 2004.

[3] P. Hasler and D. V. Anderson. Cooperative analog-digital signal processing. In *Proceedings of the IEEE Conference on Acoustics, Speech, and Signal Processing*, volume 4, pages 3972 –3975, Orlando, FL, May 2002.

[4] T. He, S. Krishnamurthy, and J. Stankovic. VigilNet: An Integrated Sensor Network System for Energy-Efficient Surveillance. *ACM Transactions on Sensor Networks*, 2(1):1–38, 2006.

[5] B. Rumberg, D. W. Graham, and V. Kulathumani. Hibernets: Energy-efficient sensor networks using analog signal processing. In *Proceedings of IPSN'2010*.

[6] N. Xu, S. Rangwala, K. Chintalapudi, D. Ganesan, R. Broad, R. Govindan, and D. Estrin. A wireless sensor network for structural monitoring. In *ACM Sensys*, 2004.