Demonstration Abstract: RAMP: Accelerating Wireless Sensor Hardware Design with a Reconfigurable Analog/Mixed-Signal Platform

Brandon M. Kelly Brandon Rumberg David W. Graham Vinod Kulathumani
Spencer Clites Alex Dilello Mir Mohammad Navidi
Lane Department of Computer Science and Electrical Engineering
West Virginia University
david.graham@mail.wvu.edu

ABSTRACT

To meet the demanding requirements in the growing area of wireless sensing applications, some sensing platforms have included low-power application-specific hardware to process the sensor data for compression and pre-classification of the relevant information. While this additional hardware can reduce the overall power consumption of the system, a unique hardware solution is required for each application. To diminish this burden, we will demonstrate a reconfigurable analog/mixed-signal sensing platform. At the hardware-level, this platform consists of a reconfigurable integrated circuit containing many commonly used circuit components that can be connected in any configuration to perform sensor interfacing and ultra-low-power signal processing. At the software level, this platform provides a framework for abstracting the underlying hardware. We will demonstrate how our platform allows a developer to create applications ranging from standard sensor interfacing techniques to more complicated intelligent pre-processing and wake-up detection, without the necessity of circuit-level expertise.

Categories and Subject Descriptors

B.7 [**Integrated Circuits**]: Miscellaneous; C.3 [**Special-Purpose and Application-Based Systems**]: Real-time and embedded systems, Signal processing systems

Keywords

Analog Signal Processing; Field-Programmable Analog Array; Energy-Efficient; In-Network Processing; Sensor Networks

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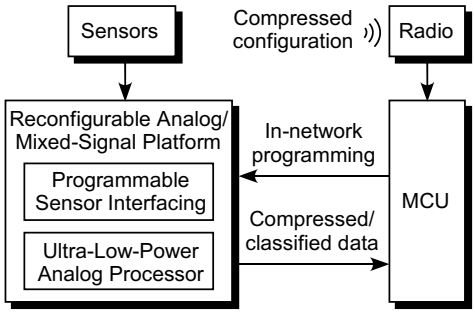

Figure 1: Architecture of a wireless sensor with reconfigurable sensor-interface hardware.

1. INTRODUCTION

The Internet of Things, wireless sensor networks, and wearable computer platforms are all low-power, sensing/computing platforms. One method for meeting their strict power budgets is the development of low-power application-specific analog front-ends for signal conditioning and pre-processing [3]. Such custom hardware can reduce the computational load of the more power-intensive digital components and also potentially reduce the amount of data which must be transmitted through the very power-intensive radio components. However, development of such hardware platforms tends to be very application-specific and also inherently limits the flexibility of the system. To solve this problem, we demonstrate a complete reconfigurable analog/mixed-signal platform (RAMP) capable of run-time reconfiguration and complex analog system implementation, within a wireless sensing architecture. The RAMP system (Fig. 1) differs from previously proposed reconfigurable platforms (e.g., [1, 4]) primarily by (1) being designed from the ground up to prototype low-power systems and (2) being a fully self-contained field-programmable mixed-signal system.

2. RAMP DESIGN

The RAMP is a field-programmable mixed-signal system which can be used to synthesize a variety of event-detection and signal-processing applications quickly and without the need for circuit-level expertise. The signal-flow inspired architecture consists of 80 computational analog blocks (CABs) arranged across ten stages in eight channels. The stages provide design components of varying granularity grouped

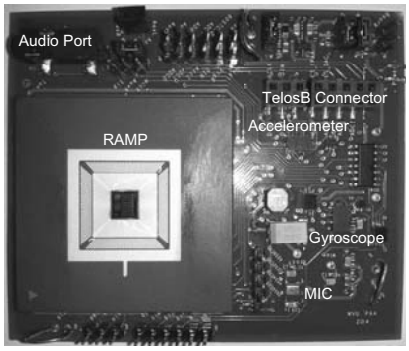

Figure 2: Development board for the RAMP.

according to function—spectral analysis, transconductors, sensor interfacing, transistors, and mixed-signal operations. The eight channels enable the architecture to process signals in parallel. The RAMP provides further design flexibility through the usage of tunable circuit parameters (e.g., filter bandwidth). These parameters are realized through the usage of floating-gate transistors as a non-volatile analog memory [2].

We have also created a development environment to simplify the design of applications on the RAMP. This development environment includes (1) a custom netlisting language to describe connections on the RAMP, (2) an automated placement routine based on simulated annealing to choose the most appropriate circuit elements, (3) an automated routing algorithm that leverages a heuristic rules-based system for connecting the basic building blocks, and (4) an abstraction framework that allows hierarchical and reusable design. These individual tools together greatly simplify the design process for the end user and help to make the device selection and connection transparent to the user.

The RAMP development board (Fig. 2) includes several sensors as well as an interface for microcontrollers. The sensors include a low-power microphone, 3-axis accelerometer, and 1-axis gyroscope. The microcontroller interface can be attached to a mote such as a TelosB or to an Arduino. This interface allows the microcontroller to receive configuration files and reprogram the RAMP as needed.

3. DEMONSTRATION

We will demonstrate in-the-field reconfiguration of the RAMP device as well as various applications that can be synthesized on it for sensor interfacing, signal processing, and event detection. These applications will make use of the sensors included on the development board to perform tasks such as orientation recognition, gesture recognition (e.g., double tap), and even a simple analog music synthesizer. More complex, yet still ultra-low-power, event-detection systems will also be demonstrated, such as a heart-rate monitor that creates an alarm if the heart rate deviates from an acceptable healthy range (Fig. 3). In addition to these applications, attendees will be able to synthesize their own applications through our development environment.

4. ACKNOWLEDGMENTS

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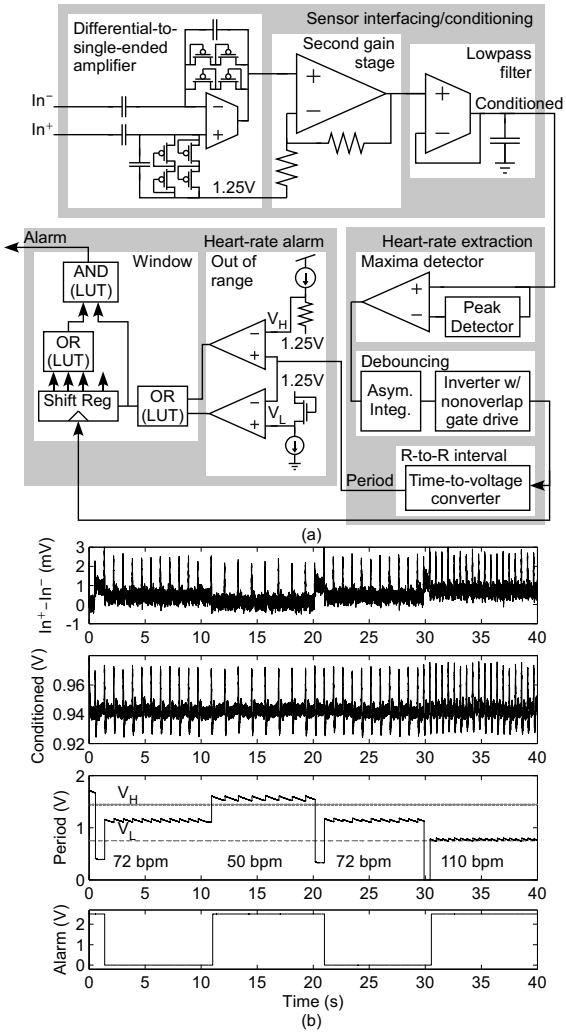

Figure 3: (a) Heart-rate monitoring system which was synthesized on the RAMP. (b) Measured response at various stages in the system. The bottom plot shows successful detection of out-of-range heart rates.

5. REFERENCES

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