SPICE-compatible modelling technique for simulating floating-gate transistors

S.J. Rapp, K.R. McMillan and D.W. Graham

A technique is introduced to enable the simulation of floating-gate transistors within standard analogue circuit simulators, such as SPICE. This technique can be used in all types of circuit simulations, ranging from DC sweeps to charge-modification scenarios. The technique is then used to simulate several analogue circuits, the results of which show strong agreement with identical circuits fabricated in standard CMOS processes.

Introduction: Floating-gate (FG) transistors, which are the core element in flash memory and EEPROM devices, consist of a standard CMOS transistor with an electrically isolated gate (Fig. 1*a*). Consequently, the gate is considered to be 'floating', and any charge on the gate will remain there indefinitely unless it is specifically modified through processes such as Fowler-Nordheim tunnelling, hot-electron injection or UV photo injection. In addition to their uses in digital memory, FG transistors have numerous applications in the analogue domain including mismatch compensation, programmable and adaptive circuits etc. However, since the gate of the FG transistor has no DC path to ground (i.e. connected only to capacitors), these useful analogue circuit elements cannot be simulated in standard SPICE circuit simulators, thus limiting the designer's ability to effectively incorporate them into working circuits.

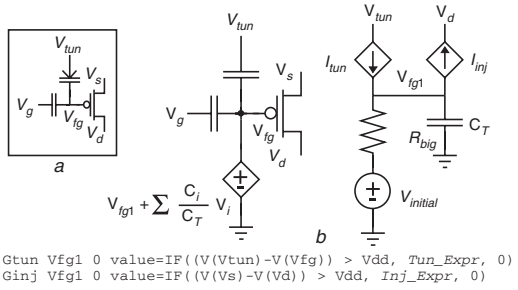

Fig. 1 *Modelling technique for FG transistors*

a Floating-gate transistor
b SPICE modelling technique

Several SPICE-compatible FG transistor models have been presented for analogue circuit applications, each of which addresses particular characteristics of FG devices. The work in [1–3] presents techniques to establish the FG voltage using capacitive coupling onto the FG node. While these techniques can provide initial charge on the FG, they provide no mechanisms to modify the stored charge during simulation. The work in [4, 5] presents models that address charge modification resulting from the previously mentioned tunnelling and injection processes. However, these models lack the ability to include capacitive coupling onto the FG node, thereby precluding their use in DC simulations and often greatly overestimating the FG transistor's output resistance. In this Letter, however, we present a SPICE-compatible modelling technique for FG transistors that can be used in all situations, ranging from DC sweeps that properly capture capacitive coupling effects to adaptive/programmable circuits that require charge modification. Moreover, this technique is flexible and extensible. Any standard SPICE transistor model can be used (e.g. BSIM, EKV, PSP) along with various models for tunnelling and injection.

Description of modelling technique: To simulate FG transistors in standard circuit simulators, such as SPICE, we have developed the technique shown in Fig. 1*b*. We use an isolated 'dummy' node for computing the appropriate amount of charge on the FG. The initial charge is established by a voltage source connected to the dummy node via a very large resistor (e.g. maximum allowable value). This large resistor aids DC convergence of the simulator, and the resulting large $R_{big}C_T$ time constant holds charge on the dummy FG node with negligible loss during transient simulations. This extra node is crucial to provide memory of the stored and/or modified charge on the FG node. Voltage-controlled current sources (VCCSs) are used to charge/discharge the dummy FG node in ways analogous to tunnelling and injection. Various models for tunnelling and injection have been developed (e.g. tunnelling [4], injection [4, 6]), and any of these models can be incorporated into these VCCSs. To permit DC convergence and DC simulations, the expressions providing I_{tun} and I_{inj} are nested within an IF statement that ensures $I_{tun} = I_{inj} = 0$ when not 'turned on' (see Fig. 1*b*). These VCCSs can be implemented using standard SPICE primitives or Verilog-A.

The actual FG voltage, V_{fg}, is established by directly connecting the FG node to a voltage-controlled voltage source (VCVS). V_{fg} is then determined by adding the stored charge from the dummy node, V_{fg1}, to a weighted average of all of the voltages coupling onto the FG node, as illustrated in Fig. 1*b*, where C_T is the total capacitance connected to the FG node, C_i is the capacitance (drawn and parasitic) between the FG and the respective terminals of the FG device, and V_i is the voltage at the corresponding terminals (V_g, V_s, V_d, V_{tun}, V_{well}). Each of the modelling parameters, including the capacitor ratios, can be obtained either from designed parameters (i.e. from layout) or from empirical fits.

Results: We have implemented our FG transistor modelling technique in several standard analogue circuit simulators (HSPICE, WinSPICE, Spectre) and have verified its operation by comparing simulation results to circuits fabricated in various standard CMOS processes. Figs. 2 and 3 show the comparisons with circuits fabricated in a 0.5 μm CMOS process, where symbols represent data from fabricated circuits and solid lines show our simulation results.

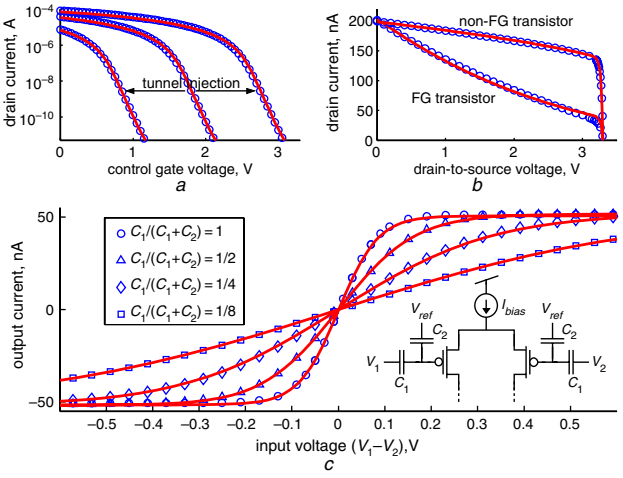

Fig. 2 *DC sweeps and capacitive coupling*

a Gate sweeps
b Drain sweeps
c Standard OTA with FG transistors as input devices

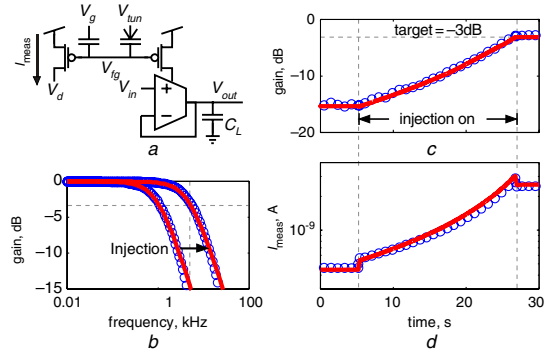

Fig. 3 *Run-time programming of lowpass filter*

a Continuous-time lowpass filter
b Before-and-after frequency response
c Programmed gain of filter
d Measured current through programmable FG transistor

Fig. 2 illustrates the use of our modelling technique to simulate DC sweeps and capacitive coupling within FG transistors. Fig. 2*a* shows DC gate sweeps of a single FG transistor with different amounts of initial charge on the FG. This modelling technique permits us to

modify the effective threshold voltage of the device, which is analogous to tunnelling or injecting the device between gate sweeps. The drain-sweep plot (Fig. 2*b*) contains data from both an FG transistor and a standard (non-FG) transistor to illustrate the importance of capacitive coupling from the drain to the the FG node, which can significantly reduce the effective output resistance of an FG transistor. Fig. 2*c* shows the results of using FG transistors as the input devices of a standard operational transconductance amplifier (OTA). Here, multiple-input FG transistors are used to extend the input linear range of the OTA by using various values of capacitive division ($C_1/(C_1 + C_2)$).

The example circuit of Fig. 3 shows that our technique can also be used to perform both charge modification and capacitive coupling onto the FG, as well as illustrating why these processes must be modelled in tandem. This circuit is a continuous-time first-order lowpass filter with a time constant that is established by the FG voltage, V_{fg}. We use the technique of run-time programming [7] to modify the charge on the FG by using tunnelling and injection while the circuit remains operational. In this example, we initiate hot-electron injection at time $t = 5$ s to slowly increase the corner frequency to 5 kHz while applying a constant input sinusoidal waveform at 5 kHz. The output signal is constantly monitored until it meets the desired objective (e.g. the output signal is -3 dB of the input signal), at which time injection is turned off and the filter continues operation at the newly established corner frequency. Injection is initiated by lowering the drain potential, V_d, of the FG transistor to provide the large source-to-drain voltage required for injection, but this change in V_d also modifies V_{fg} via capacitive coupling and potentially changes the corner frequency by a significant amount. In this example, we partially counter this resulting decrease in V_{fg} by simultaneously raising V_g, but the capacitive coupling effect is still clearly evident in the I_{meas} plot.

Conclusions: We have introduced a technique to simulate FG transistors within standard analogue circuit simulators that can be used in all types of simulations, ranging from DC sweeps to charge-modification scenarios. We also provide simulation results using our modelling technique that closely match the responses of the same circuits fabricated in standard CMOS processes.

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One or more of the Figures in this Letter are available in colour online.

S.J. Rapp, K.R. McMillan and D.W. Graham (*Lane Department of Computer Science and Electrical Engineering, West Virginia University, Morgantown, WV 26506, USA*)

E-mail: david.graham@mail.wvu.edu

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