Multiplexing high-side load switch using adaptive well biasing

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A high-side load switch is presented for applications that require multiplexing the supply terminal to multiple voltage sources that are different, unknown, and/or dynamic. The design incorporates p-channel switches with adaptive n-well biasing to ensure that no junction is forward biased. Measured results are presented from a circuit that has been fabricated in a standard 0.35 µm CMOS process. The circuit is also demonstrated in an application of programming non-volatile memory.

Introduction: As low-power electronics become more prevalent, power management is a significant concern. In low-power systems, multiple voltage sources are often used to provide supplemental energy or to reduce power consumption. Examples include switching the supply voltage from a battery to an energy-harvesting system or switching unused subsystems to a lower supply voltage. Selecting a specific voltage source to use at any given time requires a high-side load switch, which is a switch that can connect/disconnect a supply voltage to a particular load.

In a CMOS process, either an n-channel or p-channel MOSFET (nFET or pFET) can be used as a switching element. Considering that the objective of a high-side load switch is to pass a supply voltage, a pFET is a more natural choice to act as the switch even though nFETs have a better $R_{DS(ON)}$ per unit area. To achieve the same objective with nFET switches, a voltage step-up converter must be used to generate a gate voltage at least one threshold voltage above the supply voltage that is being passed; this added circuitry comes at the expense of greater silicon area, power consumption, and design complexity.

The conventional usage of a pFET-based high-side load switch is demonstrated in Fig. 1, where a load is connected/disconnected from a single supply voltage. The source and well of the single pFET are connected together to ensure that the well voltage is at the highest potential. However, this configuration poses a problem when there are multiple, differently valued, and dynamic supply voltages each coupled to the load via different pFETs. The well of each pFET switch must be connected to the highest voltage encountered, or else there is significant possibility that a well-to-diffusion junction will become forward biased, causing the high-side load switch to fail.

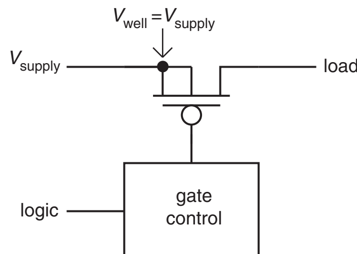

Fig. 1 *Block diagram of conventional high-side load switch*

In this work, we present a pFET-based multiplexing high-side load switch that is capable of connecting multiple supply voltages to a single load. To ensure that no junction is ever forward biased, we introduce dynamic biasing of the well potentials. This high-side load switch is capable of passing supply voltages above the rated supply voltage for a process. As a result, this circuit is able to connect the large voltages required for hot-electron injection when programming floating-gate (FG) transistors used in flash memory and analogue non-volatile memory [1], which was the original application of this high-side load switch.

While recent work on high-side switches has largely focused on using specialised processes (e.g. Bipolar-CMOS-DMOS [2, 3]), this work is focused on utilising standard devices in a CMOS process. In the following, we present the operation of the CMOS high-side load switch.

Circuit implementation: When using pFET switching elements in a high-side load switch, the wells must be biased at or near the highest potential to prevent the possibility of forward biasing. Fig. 2 displays our multiplexing high-side load switch that incorporates pFET switches along with adaptive well biasing. The adaptive well biasing occurs through the well-selection transistor pair, M_5 and M_6, by passing the higher of the two supply voltages to the common well, V_{well}. Transistors M_7 and M_8 are the switch elements that multiplex either $V_{supply1}$ or $V_{supply2}$ to the output, V_{supply_out}. Transistors M_{1-4} form a standard level shifter driven by an inverter and its complement signal; M_{1-4} and the inverter perform the function of the gate-control block of Fig. 1. The inverter should be powered either by the lowest supply or chip V_{dd}.

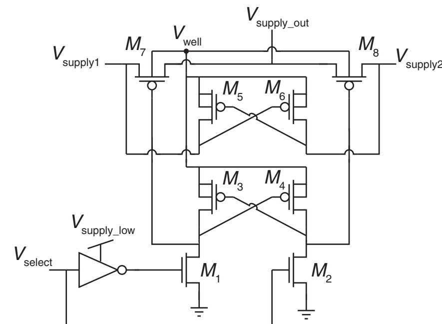

Fig. 2 *Schematic of multiplexing high-side load switch using adaptive well biasing*

The determination of which supply source is connected to the output load is specified by digital selection V_{select}. When V_{select} is high, M_2 is turned ON and the gate of M_8 is pulled towards ground, thus connecting $V_{supply2}$ to V_{supply_out}. At the same time, M_3 is turned ON and level shifts the gate of M_7 to the highest potential (i.e. n-well potential) to turn OFF the unselected switch. Recall that this n-well potential is established by the dynamic biasing from the well-selection transistor pair ($M_{5,6}$) and will be connected to the higher of $V_{supply1,2}$ regardless of the value of V_{select}. When V_{select} is low, the same, but complementary operations will occur to turn ON M_7 and turn OFF M_8.

The well-selection pair ($M_{5,6}$) has a clearly defined output when $V_{supply1,2}$ are significantly different from each other; the common well has a potential equal to the maximum of $V_{supply1,2}$. However, when $V_{supply1,2}$ are within approximately one threshold voltage (V_T) of each other, $M_{5,6}$ turn OFF, and the well voltage floats. Traditionally, this well-selection pair has been used exclusively for when $V_{supply1,2}$ are significantly different (e.g. the charge pump of [4]). However, we will describe how the well-selection pair continues to keep the high-side load switch operating as desired, even when $V_{supply1,2}$ have similar values.

When $V_{supply1} \approx V_{supply2}$, V_{well} is floating but will stay in close proximity to $V_{supply1,2}$. For instance, V_{well} cannot float higher than $V_{supply1,2} + V_T$ since that would turn ON $M_{5,6}$ and pull V_{well} back towards $V_{supply1,2}$. Also, V_{well} cannot float too low, since that would forward-bias the diffusion-to-well p-n junctions, thus adding charge to the floating well, resulting in V_{well} being pulled back towards $V_{supply1,2}$. In either scenario, V_{well} stays close enough to $V_{supply1,2}$ that there are no significant effects on the performance of the high-side load switch.

The exact value to which V_{well} floats depends on how quickly $V_{supply1,2}$ are changing. If $V_{supply1,2}$ are moving slowly (e.g. DC changes) in either the same or opposite directions, then V_{well} will settle to a value slightly less than $V_{max} = \max(V_{supply1,2})$; experimentally, we have found this voltage to be within 200 mV of V_{max}. The reason for this operation is due to the reverse-bias leakage current from the well-to-substrate pulling V_{well} down and also a slight forward-biasing of the diffusion-to-well potential for V_{max}, thus establishing an equilibrium. For faster changes in $V_{supply1,2}$, the well capacitance keeps V_{well} in close proximity to V_{max} until $|V_{supply1} - V_{supply2}| > V_T$ and V_{well} becomes strongly connected to the larger of $V_{supply1,2}$.

Results: The high-side load switch of Fig. 2 was fabricated in a 0.35 µm CMOS process using only standard 3.3 V devices (i.e. no thick-oxide I/O devices). The measured results are displayed in Fig. 3, which varies both supplies over time while switching the selection signal. Fig. 3 covers a combination of various signal situations and shows the output, V_{supply_out}, following its selected supply voltage. The middle plot shows the waveform of the common well potential, which was measured on an auxiliary circuit since this node was too sensitive to pin out; this subplot shows that the well-selection transistor pair dynamically biases

V_{well} to the highest supply voltage, and when $V_{supply1} \approx V_{supply2}$, V_{well} stays in close proximity. The experimental results also demonstrate that the circuit can safely withstand temporary voltages that exceed the rated 3.3 V supply voltage of the process. Care should be taken so that no device undergoes junction or oxide breakdown, which set the limit for V_{max}. Typically these breakdown mechanisms occur at $2\text{–}3 \times V_{dd}$ in most processes [5]; our circuit was limited to ≈ 7 V.

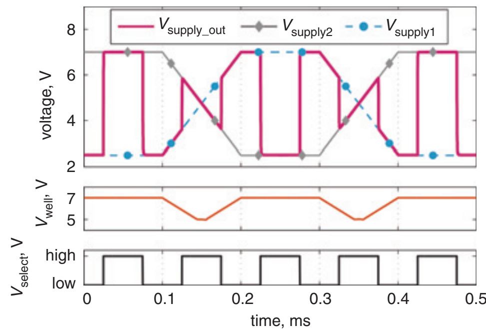

Fig. 3 *Measured results showing (top) input/output behaviour, (middle) well potential, and (bottom) selection signal. Logic high =* V_{supply_low} *and logic low = 0V*

Operation beyond the rated 3.3 V is especially useful for our target application of programming non-volatile analogue memory using FG transistors [1]. For example, hot-electron injection is a common method of precise FG programming which requires large voltages outside of the typical supply rails to create a large source-to-drain potential [6]. In this 0.35 µm process, $V_{sd} \approx 6.5$ V is required. Therefore, we temporarily enable a charge pump to generate this high voltage and use the high-side load switch to connect the FG device to the high voltage while programming. Otherwise, we connect the FG device to chip $V_{dd} = 2.5$ V. This procedure is demonstrated in Fig. 4 where a charge pump is connected to $V_{supply2}$ and is enabled at $t = 1$ s. Once the charge pump output is at 6.5 V, the high-side load switch connects V_{supply_out} (i.e. the FG transistor) to the charge-pump output ($V_{supply2}$) via V_{select}. When programming has been completed, the high-side load switch reconnects the FG transistor to chip V_{dd} ($V_{supply1}$), and then the charge pump is disabled and allowed to discharge slowly towards ground. A die photograph of this configuration is also shown in Fig. 4.

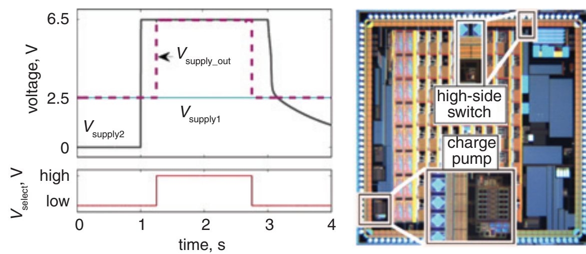

Fig. 4 *FG programming demonstration using high-side load switch and charge pump, along with a die photograph*

Measured characteristics of the multiplexing high-side load switch are displayed in Table 1. The ON-resistance of both pFET switches was measured to be 45 Ω, as designed, to meet our constraint of $R_{ON} \leq 50\ \Omega$. The ON-resistance is adjustable by sizing the switching transistor dimensions ($M_{7,8}$) to meet an application's design constraints.

Table 1: Measured characteristics

Parameter	Measurement
ON-resistance	45 Ω
rise time	10.5 ns
fall time	16.5 ns
turn-on delay time	11.5 ns
static power consumption	4.6 nW
dimensions	67 × 84 µm

Fig. 5 shows the measured power consumption of the circuit when sweeping $V_{supply2}$ and while holding $V_{supply1} = 2.5$ V. The trend can be attributed to a combination of reverse-biased p-n junction current and subthreshold leakage current. As $V_{supply2}$ decreases, the total current consumption greatly decreases, thereby reducing the static power consumption. The static power consumption of 4.6 nW shown in Table 1 was taken under the conditions of $V_{supply_low} = V_{supply1} = 2.5$ V and $V_{supply2} = 7$ V, which represents a worst-case power consumption scenario for this circuit. Note also from Fig. 5 that there is a slight increase in current when $|V_{supply1} - V_{supply2}| < V_T$. This current increase helps to validate our discussion regarding the operation of the well-selection pair ($M_{5,6}$) when $V_{supply1} \approx V_{supply2}$. When $|V_{supply1} - V_{supply2}| < V_T$, V_{well} is at a voltage between $V_{supply1,2}$. Thus, a slight forward biasing from the higher V_{supply} to the well causes current to flow into the circuit and is counteracted by a reverse-bias current flowing out of the circuit from the well to the lower V_{supply}. These currents are small and do not impact the operation of the circuit when $V_{supply1} \approx V_{supply2}$.

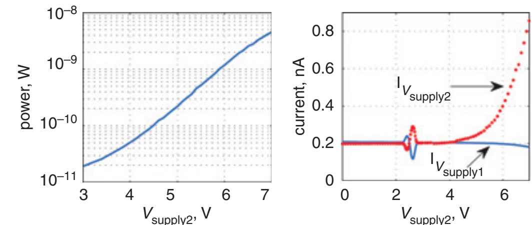

Fig. 5 *Measured power consumption and currents*

Conclusion: We have presented a multiplexing high-side load switch with adaptive well-biasing. It was fabricated in a standard 0.35 µm CMOS process. Although the rated voltage is 3.3 V, the circuit is capable of operating at a much higher supply voltage. Our load switch can serve a variety of applications, such as energy-harvesting power management and FG programming.

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One or more of the Figures in this Letter are available in colour online.

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