Demo Abstract - Netamorph: Field-Programmable Analog Arrays for Energy-Efficient Sensor Networks

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ABSTRACT

The limited power budgets of sensor networks necessitate some level of in-network pre-processing to reduce communication overhead. The low power consumption of analog signal processing (ASP) is well-suited for this task. However, the quick adoption of this technology has been restrained by the fact that ASP implementation requires *a priori* knowledge of the application space. Our solution to this challenge is to enable run-time reconfiguration through the use of a field-programmable analog array (FPAA). In the same way that reconfigurable digital systems allow system designers to change the infrastructure of digital blocks, an FPAA allows an application developer to change the infrastructure of, and even tune, ASP blocks without circuit-level expertise. We will demonstrate that an FPAA can be used to (1) facilitate the use of ASP to reduce power consumption, and to (2) allow run-time reconfigurability to maximize ASP impact.

Categories and Subject Descriptors

B.7 [**Integrated Circuits**]: Miscellaneous; C.3 [**Special-purpose and Application-Based Systems**]: Real-time and embedded systems, Signal processing systems; B.8 [**Performance and Reliability**]: Miscellaneous

General Terms

Design, Performance, Measurement

Keywords

Analog Signal Processing; Field-Programmable Analog Array; Energy-Efficient; In-Network Processing; Sensor Networks

1. INTRODUCTION

Wireless sensor networks are capable of a myriad of tasks, from monitoring the integrity of critical infrastructure such as bridges, to biomedical applications capable of monitoring a person's vital signs. However, their deployment is impractical for many applications due to their limited power budget, which is mostly spent on communication [3, 4]. In-network pre-processing can help reduce this communication overhead. As we demonstrated in [5], analog signal processing (ASP) is one form of in-network pre-processing that can be used to process a signal locally, provide event detection for wake-up scenarios, and more, all while consuming very little power. An ASP's implementation could be further improved by making the design reconfigurable, which would allow a single ASP to be used for a variety of applications and to be updated in the field as its application is redefined. To that end, we will expand upon our previous work by (1) including a field-programmable analog array (FPAA), similar to [1, 2], for added reconfigurability and by (2) utilizing an architecture that allows for more complex processing, and thus more discriminating detection.

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2. NETAMORPH DESIGN

By utilizing an FPAA locally at individual nodes (Figure 1), an application developer can easily respond to the dynamic needs of the network. The FPAA can be configured to perform various processing tasks, thus reducing the information required to be transmitted. This reduction of transmitted information is significant from a power budget standpoint, because transmission is usually characterized as one of the most power-intensive tasks of a node. Also, an FPAA can be used to characterize and detect certain events, thus creating the frame-work for a wake-up circuit. This wake-up circuit can be used to keep the power-intensive digital portion of the mote in a low-power sleep state until a predefined event is detected.

Figure 2 illustrates the use of the FPAA for a detection task. In this example, the objective is to detect when the frequency of the input signal rises from 2kHz to 4kHz. Specifically, a detection pulse should be generated when signal content is present in the 4kHz band shortly after content was present in the 2kHz band. To perform this task, the FPAA was configured such that the spectral analysis stage decomposes the signal into 2kHz and 4kHz subbands. The subband processing stages were configured to delay the output of the 2kHz band and to trigger when content was simultaneously present in the 4kHz band and the delayed version of the 2kHz band, but not present in the non-delayed version of the 2kHz band. Successful detection is shown in the bottom pane of Figure 2.

Our FPAA architecture was constructed in a standard $0.5\mu m$ CMOS process available through MOSIS and is approximately $2.25mm^2$ in area. The FPAA can be reconfigured in 100ms through a TelosB mote. The device consists of two stages: a spectral-analysis stage and a subband processing stage. The spectral analysis stage is capable of filtering and/or finding the envelope of the signal. The signal is then passed to the subband processing stage which is capable of

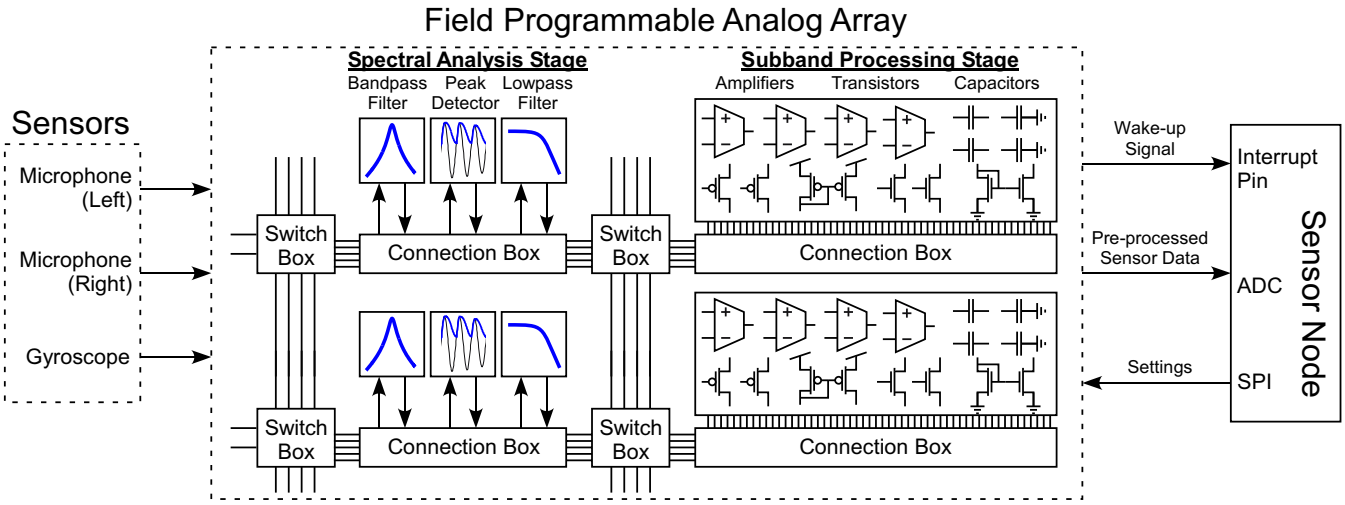

Figure 1: A sensor node equipped with a field-programmable analog array (FPAA). The FPAA can be reconfigured in run-time to perform event detection and pre-processing at a power consumption that is significantly lower than the mote's built in capabilities.

being reprogrammed to perform a myriad of tasks. In total, our FPAA has 1436 switches that can be configured to synthesize circuits with up to 40 distinct nets.

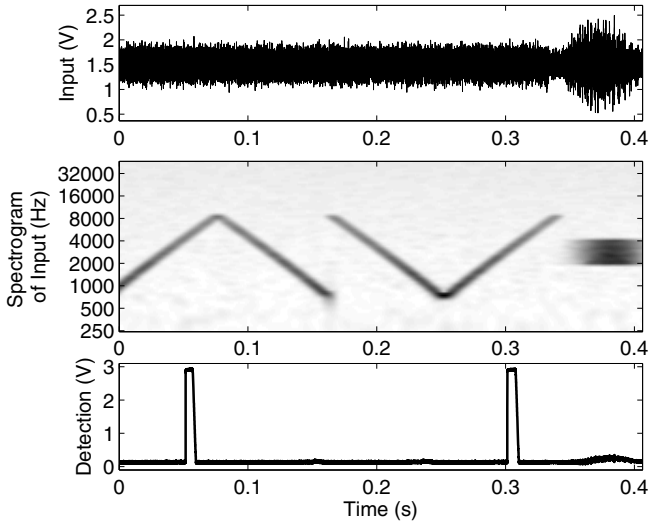

Figure 2: Example spectral analysis system implemented on the FPAA in which it is configured to detect a rising frequency in the 2-4kHz range. (Top, Middle) The input sinusoidal signal, which includes Gaussian noise, varies from 1kHz to 8kHz and concludes with an input of ten simultaneous sine waves with frequencies ranging from 2kHz to 4kHz. (Bottom) The output of the FPAA showing successful detection of the portions of the input signal where the frequency content was rising in the 2-4kHz range.

3. DEMONSTRATION

We will demonstrate the use of the FPAA for event detection and sensor pre-processing. To demonstrate these uses, we will show how a base station can send reconfiguration commands to a TelosB mote equipped with the Netamorph device. In addition to demonstrating the ability of the FPAA to implement complex signal processing tasks, we will allow conference attendees to interact with the FPAA themselves. We will demonstrate a simple user interface through which they can implement various processing tasks on the FPAA.

4. ACKNOWLEDGMENTS

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5. REFERENCES

[1] A. Basu, S. Brink, C. Schlottmann, S. Ramakrishnan, C. Petre, S. Koziol, F. Baskaya, C. M. Twigg, and P. Hasler. A floating-gate-based field-programmable analog array. *IEEE Journal of Solid-State Circuits*, 45(9):1781 –1794, Sept. 2010.

[2] E. K. F. Lee and P. G. Gulak. A CMOS field-programmable analog array. *IEEE Journal of Solid-State Circuits*, 26(12):1860 –1867, Dec. 1991.

[3] S. N. Pakzad, G. L. Fenves, S. Kim, and D. E. Culler. Design and implementation of scalable wireless sensor network for structural monitoring. *Journal of Infrastructure Systems*, 14(1):89–101, 2008.

[4] V. Raghunathan, C. Schurgers, and M. B. Srivatsava. Energy-aware wireless microsensor networks. *IEEE Signal Processing Magazine*, 19(2):40–50, Mar. 2002.

[5] B. Rumberg, D. W. Graham, and V. Kulathumani. Hibernets: Energy-efficient sensor networks using analog signal processing. In *Proceedings of IPSN*, 2010.