

Temperature Compensation of Floating-Gate Transistors in Field-Programmable Analog Arrays

Alexander Dilello[†], Steven Andryczik[†], Brandon M. Kelly[†], Brandon Rumberg[‡], and David W. Graham[†]

[†]Lane Department of Computer Science and Electrical Engineering, West Virginia University

[‡]Aspinity, Inc., Morgantown, West Virginia 26505 USA

Email: david.graham@mail.wvu.edu

Abstract—Analog pre-processing has been shown to be energy efficient in a wide variety of low-power applications. Reconfigurable analog devices have leveraged this energy efficiency and applied it to a wider application space, but they still require accurate and stable bias currents for proper operation. For single-application devices, it is sufficient to create temperature compensation schemes that apply to a single bias current. But for reprogrammable or reconfigurable platforms which can be used in a variety of applications, temperature compensation must work well over a large range of potential bias currents and for a large number of different components. In this paper, we present temperature compensation for floating-gate transistors in a reconfigurable system which improves performance over a wide range of currents and temperatures.

I. INTRODUCTION

Analog computation and pre-processing has been used in a wide variety of systems to improve energy savings, showing in some cases the equivalent of a 20-year leap in digital scaling [1]. Traditional analog pre-processing stages tend to be highly specialized application-specific systems, but developments in reconfigurable field-programmable analog arrays (FPAAs) [2], [3] have allowed these analog techniques to be applied to systems without *a priori* knowledge of the application space. One of the biggest hurdles in implementing reconfigurable analog systems lies in the infrastructure of the system. Temperature compensation is a particular challenge since the diverse application space demands a wide range of stable bias currents.

Many reconfigurable analog systems utilize floating-gate (FG) transistors to provide programmable bias currents [2], [3]. Unfortunately, the programmable bias currents generated by FG transistors are quite sensitive to temperature. There have been some successes in implementing temperature compensation for FGs employing large passive devices; however, these techniques are too area-hungry to be a viable option in dense FG arrays [4]. Others have employed a varactor on the FG node and use an additional voltage to modulate the capacitance at the FG node in response to temperature effects [5], [6]. This varactor-based method has been implemented on-chip and off-chip with great success, but has only been demonstrated for a temperature range between 25 – 43°C due to the small tuning range of the varactor. Moreover, no work has yet demonstrated the ability of a temperature compensation circuit to accurately regulate a multitude of currents across an array of floating-gates, as would be utilized by an FPAA system, without adding unfeasible levels of power or area overhead.

Portions of this material were based upon work supported by the National Science Foundation under Award Number 1148815 and by the Department of Energy National Energy Technology Laboratory under contract DE-FE0012383.

This work explores temperature compensation of FG transistors when the required number and values of currents remain unknown at design time. All plots depict measured results from an integrated circuit fabricated in a standard 0.35μm CMOS process.

II. FLOATING-GATE DEVICES

FG devices are most commonly implemented as flash memory in digital systems, but they also have a memory-like application in analog systems. Within the context of analog systems, floating-gate devices can be programmed to hold a specific amount of charge on the gate, which is electrically isolated by a coupling capacitor. By programming specific amounts of charge on the gate, and thus programming the channel current to a specific value, the FG transistor becomes a tunable current source.

FPAAs often utilize large arrays of these FG devices [2], [3]. Within the FPAA system in this work, there are over 300 biases realized by FGs which control elements ranging in granularity from current-starved inverters to bandpass filters. This wide range of elements necessitates a vary wide range of bias currents — creating a need for a temperature compensation circuit which can stabilize a wide range of currents.

Before operating an FG device as a current source, it must first be programmed. There are two common programming mechanisms for modifying charge on an FG: Fowler-Nordheim (FN) tunneling and hot-electron injection. FN tunneling is typically used as a global erasure for all FGs since it is difficult to tunnel individual FGs. The procedure for FN tunneling is accomplished by significantly increasing the tunneling node capacitor (referred to as V_{tun} in Fig. 2). Under these conditions, charge is drawn off the FG node. Hot-electron injection is typically used to add electrons to the FG. This is accomplished by raising the FG transistor's V_{DD} to generate drain current conditions favorable for impact ionization. The 'hot electrons' with enough energy to surmount the FG barrier contribute electrons to the FG.

A transistor's operational characteristics will have an inherent dependence on temperature. Furthermore, transistors operating in the sub-threshold region, which is our main application operation area, experience more extreme changes (exponential) in channel current for a change in temperature than when in above-threshold operation.

Figure 1 shows the extent of temperature effects on an FG transistor. This example demonstrates for a single programmed FG device with a fixed V_{cg} — the voltage node for setting the target current bias — that the output current wildly varies with temperature change. Holding V_{cg} constant is the traditional

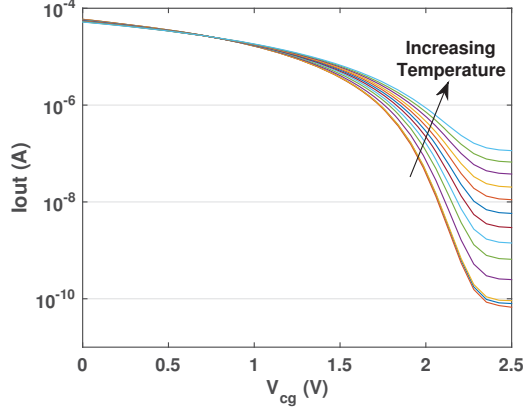


Fig. 1. Temperature dependence of a FG transistor. The plateaued currents for $V_{cg} > 2.25V$ are artifacts of many junction connections to a single global connection where the current reading was taken. As a consequence, their collective leakage current becomes non-negligible and is manifested in these measurements. The current in a single FG transistor continues below these values.

method for setting target bias currents in FPAA; however, a compensation circuit to modify V_{cg} in response to a change in temperature is clearly needed.

To generate temperature compensation, we use an FG current multiplier, as illustrated in Fig. 2 [6]. Considering that M_{REF} and M_1 have the same W/L , the charge stored on their respective FGs can be modified and used to ratio the reference current I_{REF} to I_{M1} . Operating an FG in the sub-threshold saturation region can be characterized by the following:

$$I_d = I_o e^{-q\kappa V_{fg}/kT} e^{qV_s/kT} e^{V_d/V_A} \quad (1)$$

where all voltages are referenced to the well potential, V_{fg} is the FG voltage, V_A is the Early voltage, and $q\kappa/kT$ defines the subthreshold current slope with kT/q being the thermal voltage (k = boltzmann constant). V_{fg} can be approximated as:

$$V_{fg} = \frac{Q_{FG}}{C_T} + \frac{C_{cg}}{C_T} V_{cg} + \sum \frac{C_{par}}{C_T} V_x \approx \frac{Q_{FG}}{C_T} + \frac{C_{cg}}{C_T} V_{cg} \quad (2)$$

where Q_{FG} is the amount of charge on the FG, C_T is the total capacitance seen at the FG node including parasitic capacitances, C_{cg} is the control gate capacitance, and C_{par} are the parasitic capacitances with V_x being the terminal voltages coupled to V_{fg} . The right-hand side is a reasonable approximation given that C_{cg} represents the majority of total capacitance C_T . Then, incorporating (1) and (2) into the FG current multiplier topology of Fig. 2 renders the following output current relationship:

$$I_{M1} \approx I_{REF} \exp \frac{q\kappa(Q_{M_{REF}} - Q_{M1})}{C_T kT} \quad (3)$$

where $Q_{M_{REF}}$ and Q_{M1} signifies the amount of charge on their respective FGs. Equation (3) shows that all temperature dependence is removed from the output current for charge-matched FGs in the mirror topology. For FGs with unmatched charges in the mirror, there still exists a temperature dependence, but its effects are greatly diminished compared to an FG without temperature compensation. Unmatched charges have a temperature dependence that can be characterized for the following two cases: $Q_{M1} < Q_{M_{REF}}$ and $Q_{M1} > Q_{M_{REF}}$,

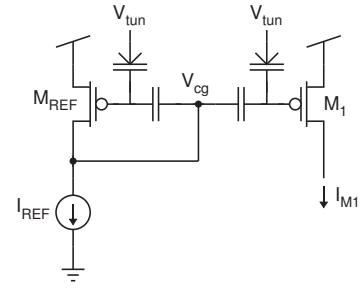


Fig. 2. Floating-gate current mirror.

where a larger charge amount is the result of fewer electrons on the FG and will correspond to a smaller current. Defining the exponential terms in (3) as β with the exception of T

$$\beta = \frac{q\kappa(Q_{M_{REF}} - Q_{M1})}{kC_T} \quad (4)$$

gives the following expression of I_{M1} for the two differing charge cases:

$$I_{M1} = \begin{cases} I_{REF} e^{\beta/T} & Q_{M1} < Q_{M_{REF}} \Rightarrow I_{M1} > I_{REF} \\ I_{REF} e^{-\beta/T} & Q_{M1} > Q_{M_{REF}} \Rightarrow I_{M1} < I_{REF} \end{cases} \quad (5)$$

Taking the derivative of (5) with respect to temperature yields a negative temperature relationship for $I_{M1} > I_{REF}$ and a positive relationship for $I_{M1} < I_{REF}$

$$\frac{dI_{M1}}{dT} = \begin{cases} -\frac{I_{REF}\beta}{T^2} e^{\beta/T} & Q_{M1} < Q_{M_{REF}} \\ \frac{I_{REF}\beta}{T^2} e^{-\beta/T} & Q_{M1} > Q_{M_{REF}} \end{cases} \quad (6)$$

These temperature coefficients will be manifested in the current measurement slope over a temperature range and become more apparent with larger differences in charge.

III. FG TEMPERATURE COMPENSATION

The application presented in this paper is applied to our FPAA, which is called the Reconfigurable Analog and Mixed-signal Platform (RAMP) [2]. To provide temperature compensation to such a large-scale system, we are leveraging the FG current mirror shown in Fig. 2. As stated in Section II regarding FPAA, the RAMP utilizes floating-gates to provide precise, but temperature-dependent current sources. The FG current mirror is used to generate a control gate (V_{cg}) voltage that responds to changes in temperature and reduces its effect on current variation.

A. System Architecture

Our RAMP includes over 300 controllable current sources generated from FGs to be used as biases for the different circuits included within the RAMP. As an FPAA, the RAMP utilizes ‘‘Computational Analog Blocks,’’ or CABs, as building blocks for post-fabrication reconfiguration. The CABs can include simple devices or full circuits. By routing the CABs together and making connections to the FG biases, analog and mixed-signal systems can be synthesized directly on the RAMP. Figure 3 shows a block-level diagram of the RAMP and how the bias currents, as well as how temperature compensation fits in to the system as a whole.

To implement the FG current mirror for temperature compensation, a ‘‘reference’’ transistor is set-up in diode connection

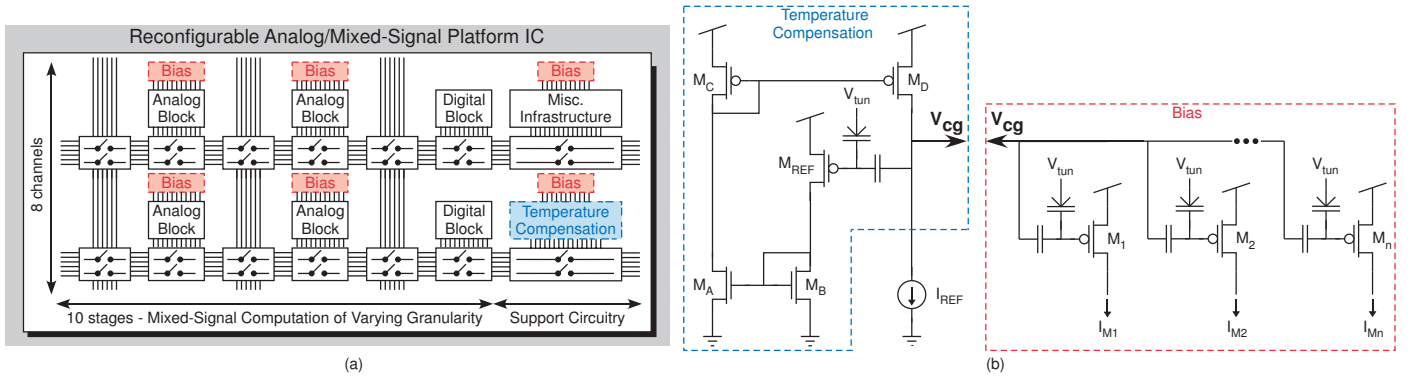


Fig. 3. (a) FPAA block diagram showing the position of the specialized CAB which houses the FG temperature compensation structure. (b) Floating-gate temperature compensation structure showing connection to global V_{cg} . Currents $I_{M1} - I_{Mn}$ source to an nFET current mirror before connecting to the CAB circuits.

to dynamically set the global V_{cg} so that a steady current will be seen on any other FG connected to the mirror topology. To accomplish this, a specific CAB has been added to the RAMP that allows for the diode connection. Figure 3 shows the full schematic of the compensation circuit within a floating-gate array. Transistor M_{REF} is placed in diode connection via the current mirrors comprised of transistors M_A - M_D . Transistor M_D mimics the behavior of the M_{REF} , specifically at its drain. All reference transistors are sized identically to ensure the same current flowing from the drain of M_{REF} is also flowing from the drain of M_D . The drain of M_D is then connected to the global V_{cg} node, allowing for the complete diode connection of M_{REF} .

This topology employing two current mirrors out of the reference FG transistor is used instead of a simple diode connection (i.e. drain connected to the control gate) to ensure that the drain of M_{REF} is kept at a relatively fixed potential. With a conventional diode connection, any fluctuations at the drain of the reference transistor would be parasitically coupled to the floating-gate as indicated by (2), causing potentially large fluctuations in channel current. By using the current mirrors to create the diode connection, the voltage seen at the drain of the reference transistor will be more constant. A similar method is employed with the FGs used as current references. Instead of connecting the FG directly to a circuit as a bias, a single nFET-based current-mirror is used to ensure that any fluctuations in the circuit will not affect the FG output.

B. System Programming

The first crucial step in programming our temperature compensation system is to determine a value of I_{REF} . I_{REF} is the stable, temperature-independent, reference current which the rest of the system will refer to as the temperature of the environment fluctuates. The closer I_{REF} is to the individual mirrored current values, the more accurately the system will be able to compensate. For this demonstration within the RAMP system, we chose a value typical of low-power analog bias currents – $10nA$. Generally, this choice should be made by matching I_{REF} to the average value of the expected currents of M_1 - M_n or the current which is most sensitive to temperature that is being implemented in the design.

For a given I_{REF} , when M_{REF} is programmed and diode connected, a particular V_{cg} will occur. With a known value of V_{cg} , we can characterize the programming of M_1 - M_n .

The programming is controlled by a continuous-time feedback circuit, similar to the one presented in [7]. The continuous-time programmer injects the FG to some value dependent upon a user-specified target voltage. At a given V_{cg} , this FG value will generate some specific current in M_n which can be stored in a look-up table to relate the value of the programmer’s target voltage to the resultant current in M_n for a given V_{cg} . We can then use this look-up table to program the currents of M_1 - M_n to any specified value.

A comparative view on the effectiveness of temperature compensation is demonstrated in Fig. 4. This shows the temperature compensation performance relative to the room temperature programming target from -25 to $85^\circ C$. Each line in Fig. 4(a) corresponds to a different ratio between the current I_{REF} and the current flowing through transistor M_n (depicted in Fig. 3(b)). The current I_{Mn} was programmed at room temperature ($25^\circ C$) and adjusted via the FG temperature compensation structure shown in Fig. 3.

The large variance in current ratios shown in Fig. 4 is a constraint imposed by the nature of the RAMP, allowing for the device to span a wide range of applications without limiting the range of available bias currents. The best case is when the current targets between the FG (M_n) and FG reference (M_{REF}) are equal. As predicted by (3), ratios other than 1 : 1 will result in less temperature compensation. With these ratios, which are a result of differing FG charges, a positive (negative) trend versus increasing temperature is the result of a negative (positive) difference in the numerator of (3). However, despite not working as well as a 1 : 1 ratio, these cases still perform better than an uncompensated scenario, as shown in Fig. 4(c).

IV. SYSTEM PERFORMANCE

Figure 1 shows the exponential dependence of temperature effects on uncompensated FGs. Due to the nature of the RAMP, target currents used for the operation of specific, synthesized circuits will be unknown until the end-user picks a desired application. Subsequently, depending on the complexity of the synthesized design, there will be more than one target current, at more than one target value. This calls for the ability to apply temperature compensation for a wide range of FG injection targets from a single targeted I_{REF} .

To show the advantage of temperature compensation in the RAMP system, a current-controlled ring oscillator has been

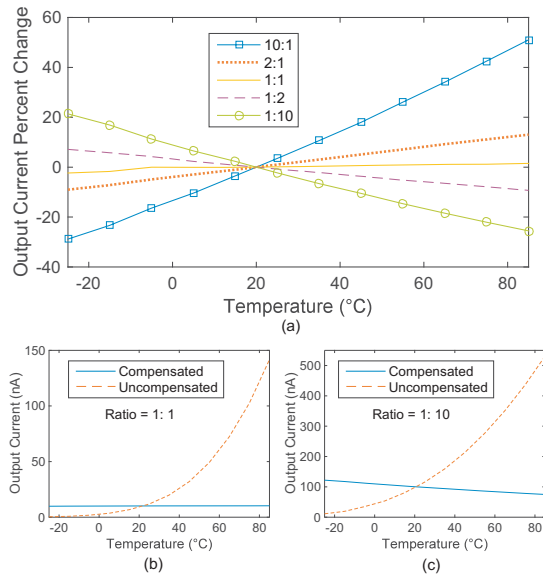


Fig. 4. (a) Percent change in output current of an FG with temperature compensation normalized to room temperature. (b) and (c) show the effects of compensation compared to an uncompensated case for a ratio of 1:1 and 1:10 respectively.

synthesized from one of the CABs. This circuit utilizes an input current, I_{in} (generated by one of the FGs) to starve its odd number of inverters, producing output frequency oscillations proportional to the input current (Fig. 5(a)). For an output frequency of 10kHz, I_{in} was set to $33nA$. The I_{REF} current chosen for the temperature compensation system was set at $20nA$. Utilizing a ratio of 1 : 1.65 for I_{REF} and I_{in} , the compensation scheme is able to decrease the fluctuations of the bias current over the temperature sweep of 0 – $90^{\circ}C$.

The ring oscillator was tested with both an uncompensated and temperature-compensated FG. The oscillator output frequency for both cases is shown in Fig. 5(a). The current bias using an uncompensated FG changes exponentially with increasing temperature while the compensated current bias remains close to the same value for the full temperature sweep.

A synthesized comparator example is shown in Fig. 5(b). The FG is programmed to draw a current across a resistor to set a desired reference voltage level, V_{REF} . The uncompensated and compensated V_{REF} measurements are shown in Fig. 5(b) where the reference current was set to $10nA$ and the current through the resistor was programmed to be $100nA$ for a ratio of 1 : 10. The temperature compensation ratio does not represent an ideal case, but greatly outperforms the uncompensated case.

V. CONCLUSION

A temperature compensation circuit was presented for FG-dense structures such as an FPAA to improve performance over a temperature-varying environment. It is able to compensate for a multitude of FG biases with various output currents, which is representative of the variable nature of FPAA usage. The compensation system has been demonstrated to work with an array of FG current sources intended for biasing components such as an oscillator or other analog blocks. Its performance

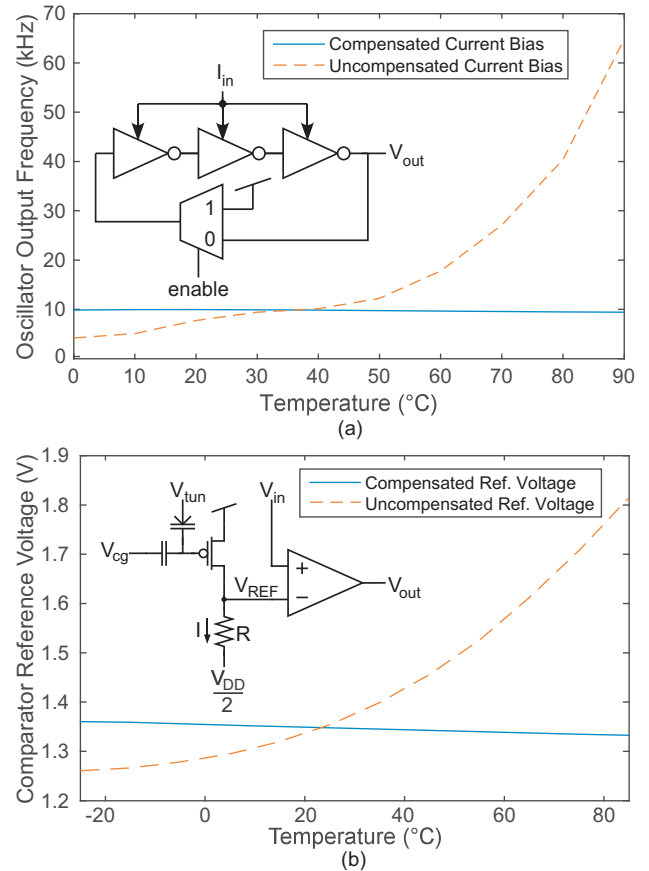


Fig. 5. (a) Ring oscillator frequency output with respect to temperature for a compensated and uncompensated FG current bias. (b) Programmed comparator reference value with respect to temperature for a compensated and uncompensated FG current bias.

has been tested as a part of the larger FPAA system and shown to improve current bias stability.

REFERENCES

- [1] S. Ravindran, P. Smith, D. Graham, V. Duangdom, D. Anderson, and P. Hasler, "Towards low-power on-chip auditory processing," *EURASIP J. Applied Sig. Process.*, vol. 2005, no. 7, pp. 1082–1092, May 2005.
- [2] B. Rumberg, D. Graham, S. Clites, B. Kelly, M. Navidi, A. Dilello, and V. Kulathumani, "RAMP: Accelerating wireless sensor hardware design with a reconfigurable analog/mixed-signal platform," in *Proc. of ACM/IEEE Inform. Process. in Sensor Networks*, 2015, pp. 47–58.
- [3] A. Basu, S. Brink, C. Schlottmann, S. Ramakrishnan, C. Petre, S. Koziol, F. Baskaya, C. M. Twigg, and P. Hasler, "A floating-gate-based field-programmable analog array," *IEEE J. Solid-State Circuits*, vol. 45, no. 9, pp. 1781–1794, Sept. 2010.
- [4] V. Srinivasan, G. Serrano, C. M. Twigg, and P. Hasler, "A floating-gate-based programmable CMOS reference," *IEEE Trans. Circuits Syst. I*, vol. 55, no. 11, pp. 3448–3456, Dec. 2008.
- [5] M. Gu and S. Chakrabarty, "Subthreshold, varactor-driven CMOS floating-gate current memory array with less than $150\text{-ppm}^{\circ}k$ temperature sensitivity," *IEEE J. Solid-State Circuits*, vol. 47, no. 11, pp. 2846–2856, Nov. 2012.
- [6] L. Zhou and S. Chakrabarty, "A continuous-time varactor-based temperature compensation circuit for floating-gate multipliers and inner-product circuits," in *IEEE Int. Symp. on Circuits and Syst.*, May 2015.
- [7] B. Rumberg and D. Graham, "Sub-microwatt analog VLSI trainable pattern classifier," *Proc. IEEE MWSCAS*, pp. 214–217, Aug 2012.