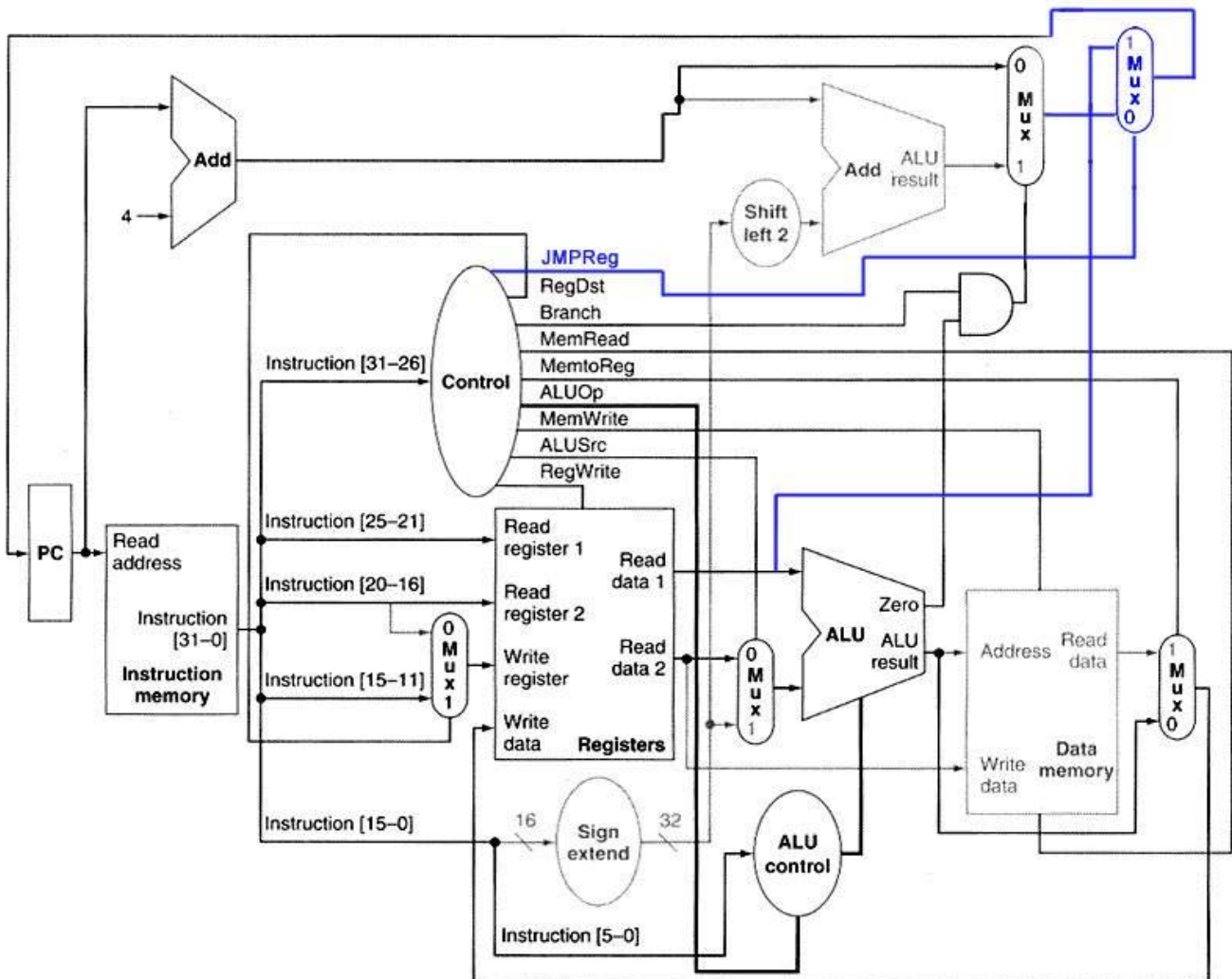


SOLUTIONS FOR ASSIGNMENT # 3

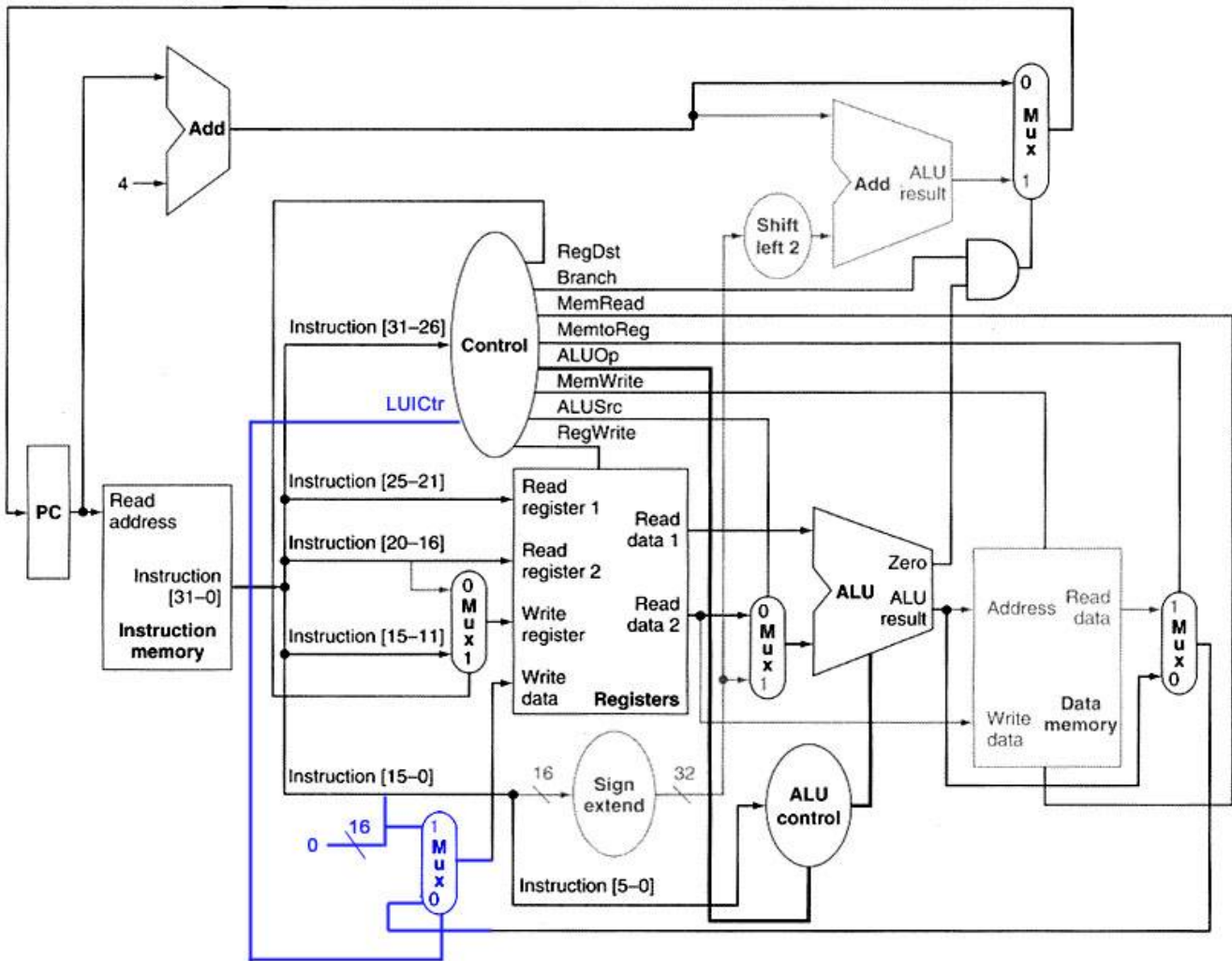
Chapter 5 Problems 5.8, 5.10, 5.13, 5.28

5.8 Show the needed changes to the single cycle processor design of MIPS shown below to support the jump register instruction JR of the MIPS instruction set architecture.



Instr	RegDst	ALUSrc	Mem toReg	Reg Write	Mem Read	Mem Write	Branch	ALUOp 1	ALUOp 2	JMPReg
R-type	1	0	0	1	0	0	0	1	0	0
lw	0	1	1	1	1	0	0	0	0	0
sw	x	1	x	0	0	1	0	0	0	0
beq	x	0	x	0	0	0	1	0	1	0
jr	x	x	x	0	x	0	0	x	x	1

5.10 Show the needed changes to the above single cycle processor design of MIPS shown below to support the load upper immediate LUI instruction of the MIPS instruction set architecture.



Instr	RegDst	ALUSrc	Mem toReg	Reg Write	Mem Read	Mem Write	Branch	ALUOp 1	ALUOp 2	LUICtr
R-type	1	0	0	1	0	0	0	1	0	0
lw	0	1	1	1	1	0	0	0	0	0
sw	x	1	x	0	0	1	0	0	0	0
beq	x	0	x	0	0	0	1	0	1	0
lui	0	x	x	1	x	0	0	x	x	1
LUI (ALT)	0	1	0	1	x	0	0	1	1	

Alternatively the other solution (LUI ALT) would not require any changes to the data path and would feed the zero extended (Extend=0) of Instruction[15-0] to the second input of the ALU (ALUSrc=1), set the ALUOp bits=11 for a logical 16-bit left shift operation at the ALU specified by the ALU control, then set MemtoReg=0, set RegWrite=1 and set RegDst=0 to write the ALU result to Reg Rt.

5.13 Consider the above cycle processor design of MIPS, a friend is proposing to modify it by eliminating the control signal MemtoReg. The multiplexer that has the MemtoReg as an input will instead use either the ALUSrc or the MemRead control signal. Will your friend's modification work? Can one of these two signals (MemRead and ALUSrc) substitute for each other? Explain.

For the first question, using MemRead instead of MemtoReg is fine since the first is only asserted for lw instructions and the second is asserted for the lws also when output data lines from memory is to be connected to the Write Data lines of the register file. This is not the case for ALUSrc since this is asserted for I-type instructions also as well as the memory access instruction.

The second question, can one of the two signals (MemRead and ALUSrc) substitute for one other?

No It is not possible to substitute ALUSrc for MemRead because of the I type instructions such as ori.

5.28 The concept of the "critical path", the longest possible path in the machine, was introduced in 5.4 on page 315. Based on your understanding of the single-cycle implementation, show which units can tolerate more delays (i.e. are not on the critical path), and which units can benefit from hardware optimization. Quantify your answers taking the same numbers presented on page 315

The concept of the "critical path", the longest possible path in the machine, was introduced in 5.4 on page 315. Based on your understanding of the single-cycle implementation, show which units can tolerate more delays (i.e. are not on the critical path), and which units can benefit from hardware optimization. Quantify your answers taking the same numbers presented on page 315.

Longest path is load instruction (instruction memory, register file, ALU, data memory, register file). It can benefit by optimizing the hardware.

Using the numbers from pg 315

Mem units: 200ps
ALU&Adders: 100ps
Register File: 50ps

Critical path = $200+50+100+200+50 = 600ps$ (for lw)

The path between the adders and the pc can tolerate more delays because they do not lie within the critical path. Any unit within the critical path (ALU, Register, Data memory) would benefit by optimizing the hardware, this would make the critical path shorter