Analog IC Layout

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Overview

- CMOS processes are constructed from “mask” sets
- Each mask represents the information for a specific layer
- Each layer contains all the shapes of a specific material (e.g. polysilicon, diffusion regions, metal, etc.)
  - Layers are stacked one on top of each other
  - Layers will not touch other layers unless specified to do so
- To create an actual design that can be fabricated, we must specify/draw the shapes for each layer

Layers

- Each layer represents a specific type of material for a specific purpose
- Examples include
  - Diffusion regions – for sources and drains
  - Polysilicon – for gates
  - Metal layers – for routing/interconnections (typically several independent metal layers)
  - Contacts – connecting MOSFET terminals to the lowest metal layer (metal 1)
  - Vias – connecting from one metal layer to the next higher or lower metal layer

Design Rules

- Design rules specify minimum requirements to ensure reliability when fabricated
- Examples include
  - All contacts must be a specific size
  - Minimum transistor W and L
  - Minimum spacing between metal lines in the same metal layer
- Design Rules Check (DRC) – IC design tools will check to ensure that all minimum requirements have been met
- Your design must pass DRC before a foundry will fabricate your design

Extraction

- Netlist extraction will translate your design shapes into actual components for verification purposes
- Can use extracted layout to
  - Resimulate your design
    - Verify operation that it works
    - Determination of parasitics
  - For comparison with your schematic (layout vs. schematic checks)

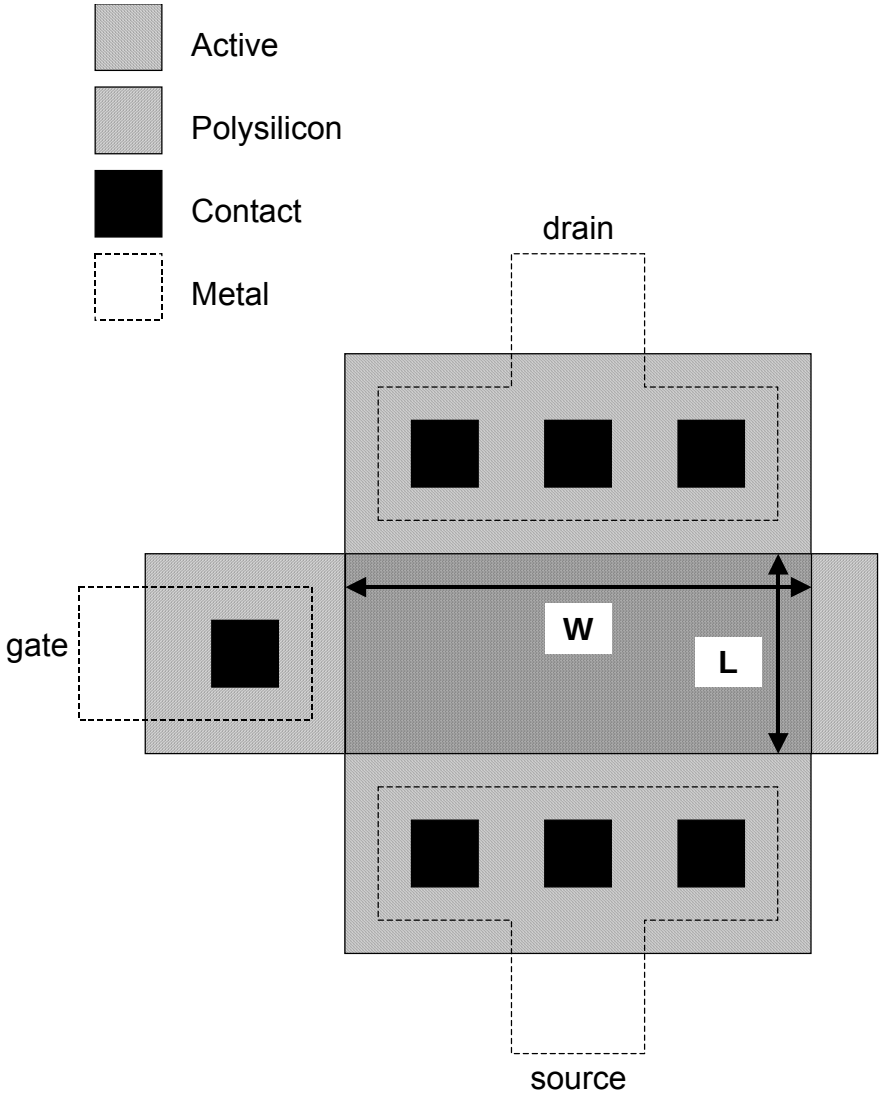
Layout vs. Schematic (LVS)

- Layout vs. Schematic (LVS) verification
  - Comparison of your schematic with the netlist extracted from your layout
  - A critical verification step!
- This verification step can be time consuming (if you have multiple errors in your layout)

Unit Sizes

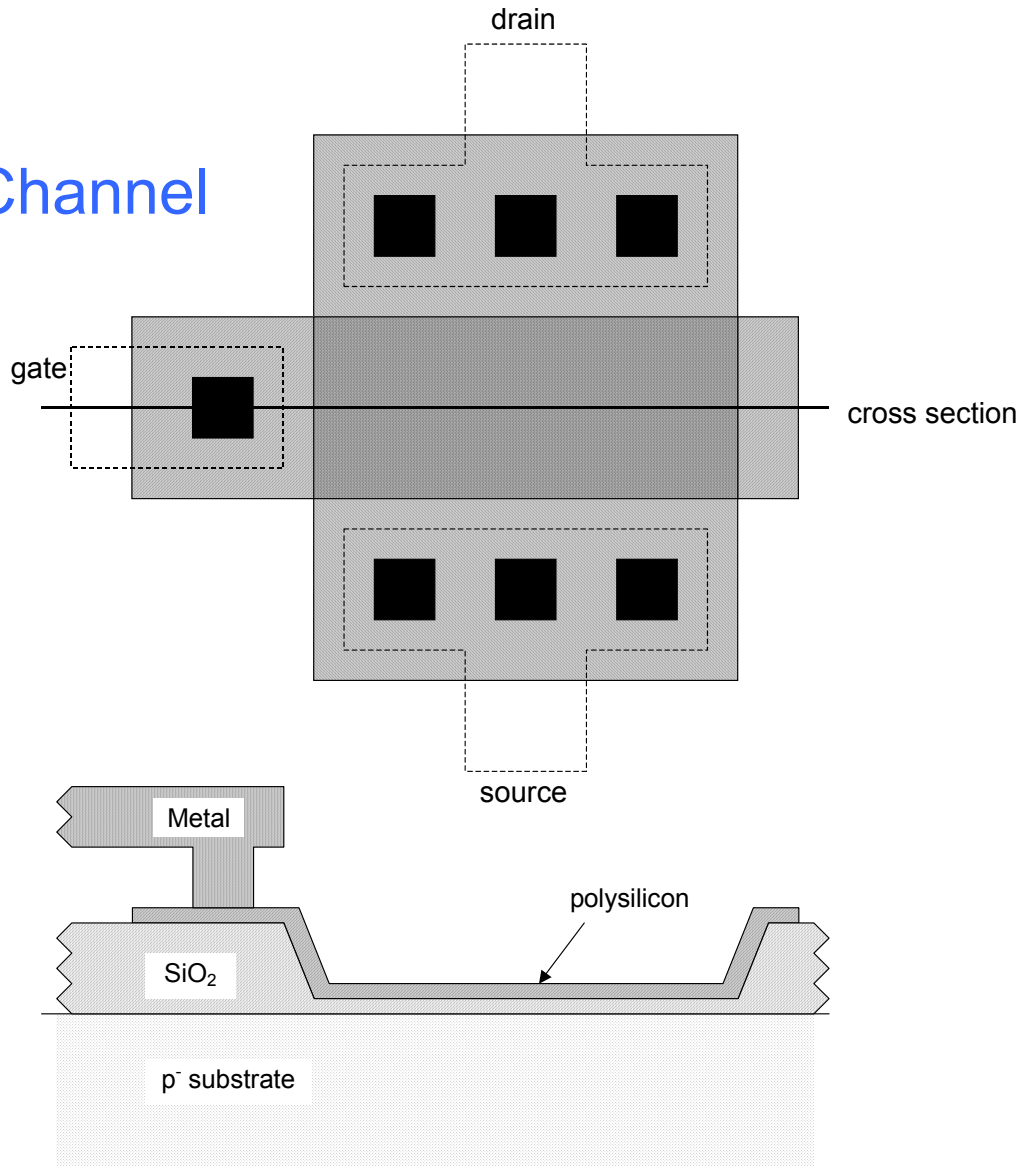
- Grid size/spacing
  - Layout has a minimum size/resolution which can reliably be fabricated on a specific process
  - Smallest quantized size
  - All drawn dimensions are scalar multiples of this size
  - Similar to “snap-to”
- Exact dimension vs. lambda
  - Layout can be specified in exact sizes (i.e. μm)
  - Layout can be specified in relative sizes (i.e. λ)
  - λ is used with “scalable” CMOS processes
    - Provides general rules for all CMOS processes
    - Moving a design to a new process requires no additional modification to the design
    - λ is mapped to a specific size for the process – everything else is scaled accordingly
    - Harder to use for submicron processes (too many “new” rules)
    - Ex. minimum transistor length is 2λ (λ = 0.3μm in a 0.5μm process)

nFET Layout



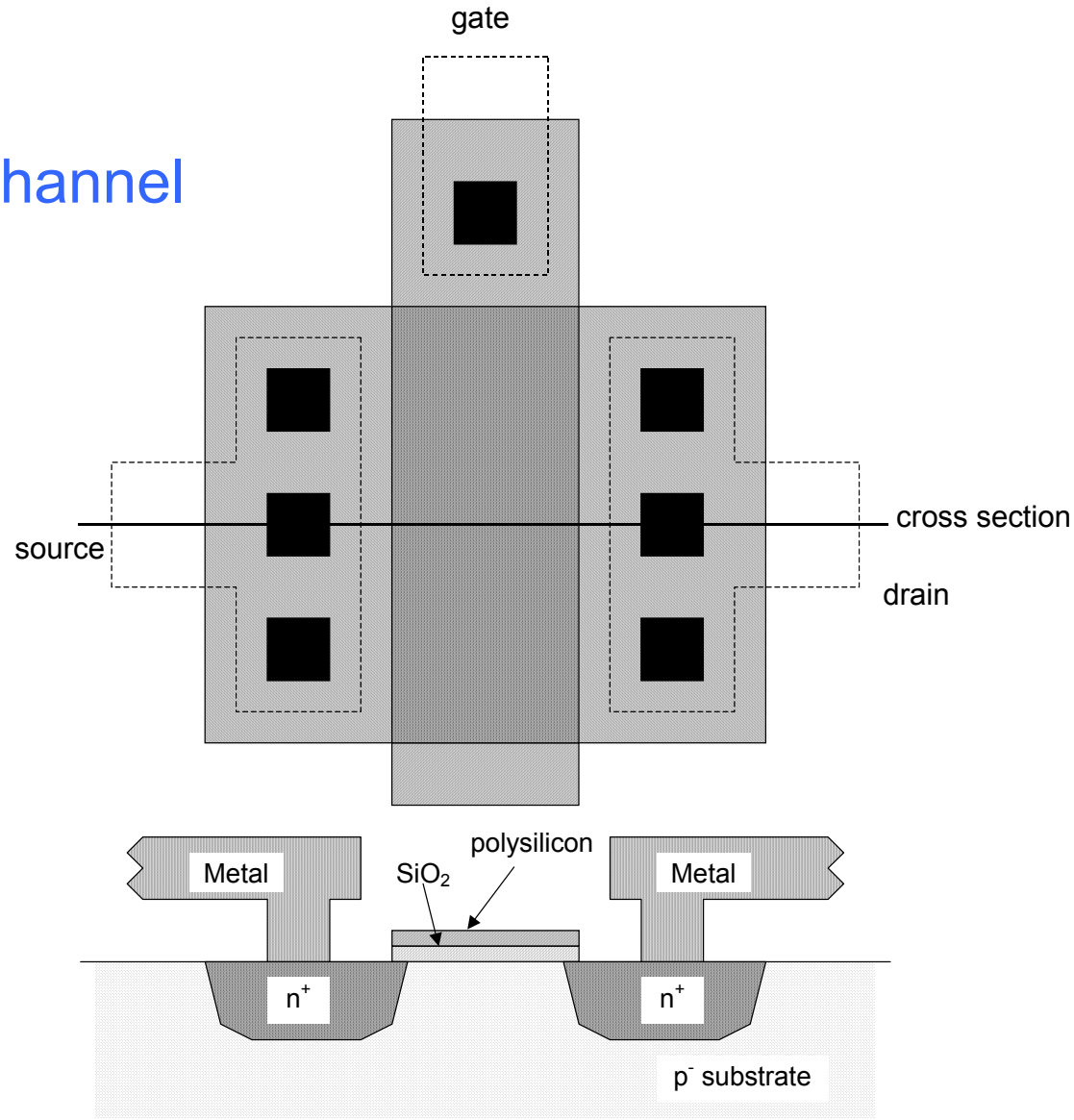
nFET Cross Sectional View

Across the Channel



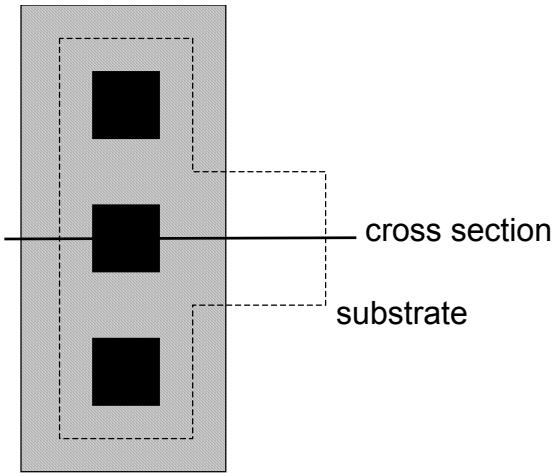
nFET Cross Sectional View

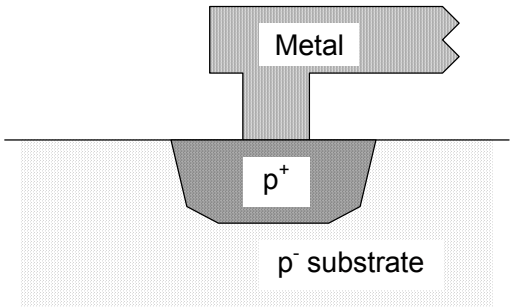
Along the Channel



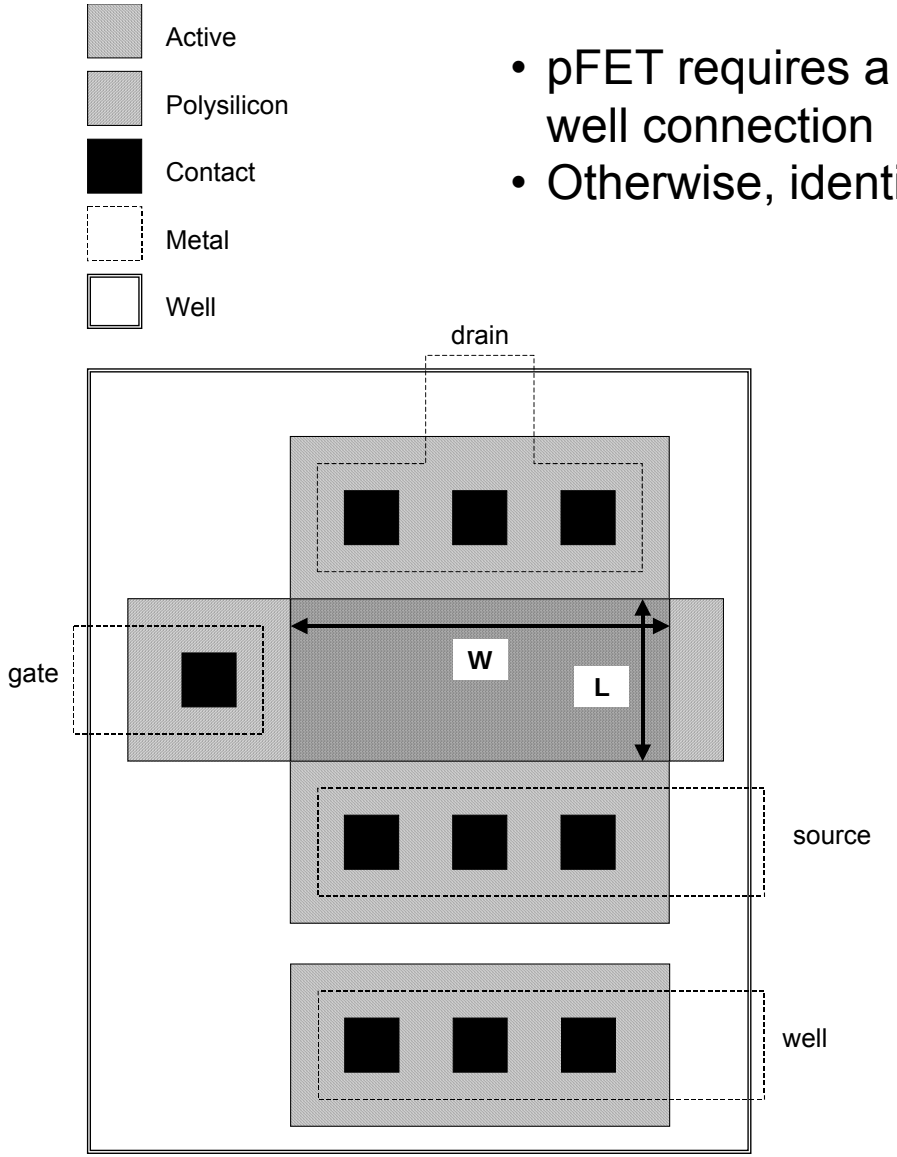
Substrate Connection

The bulk is the fourth terminal
Do not forget to tie down the bulk



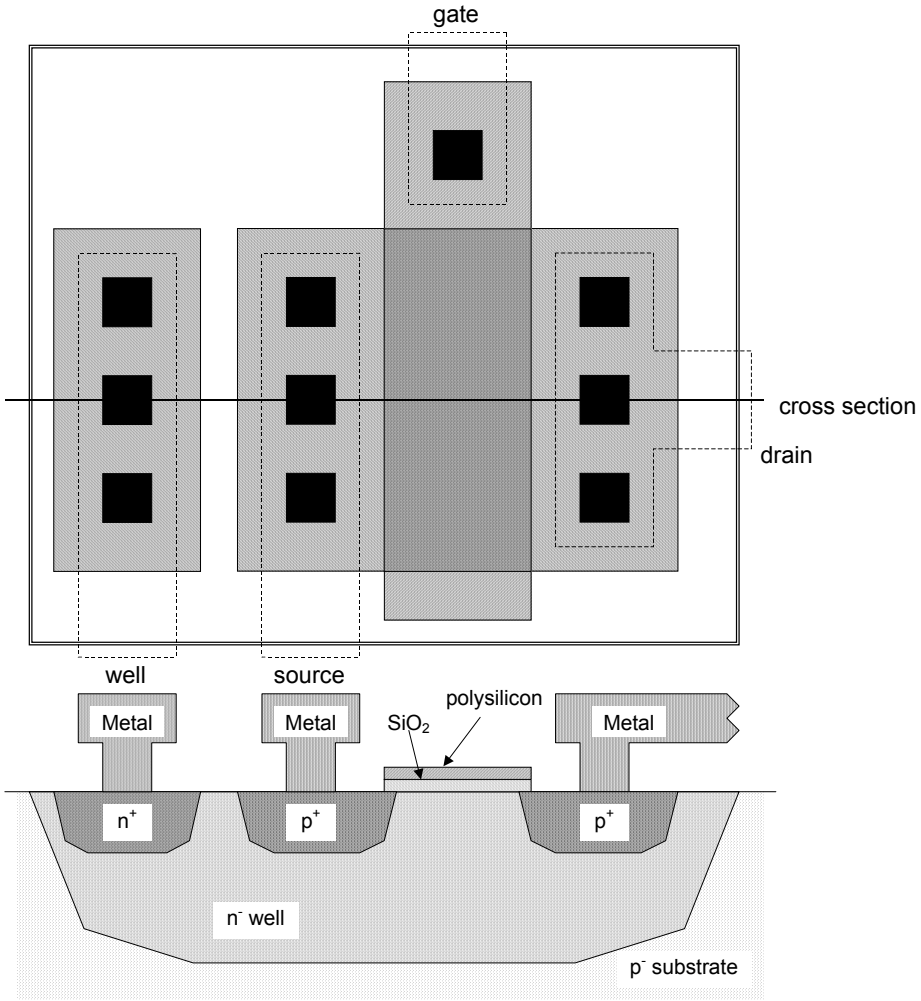


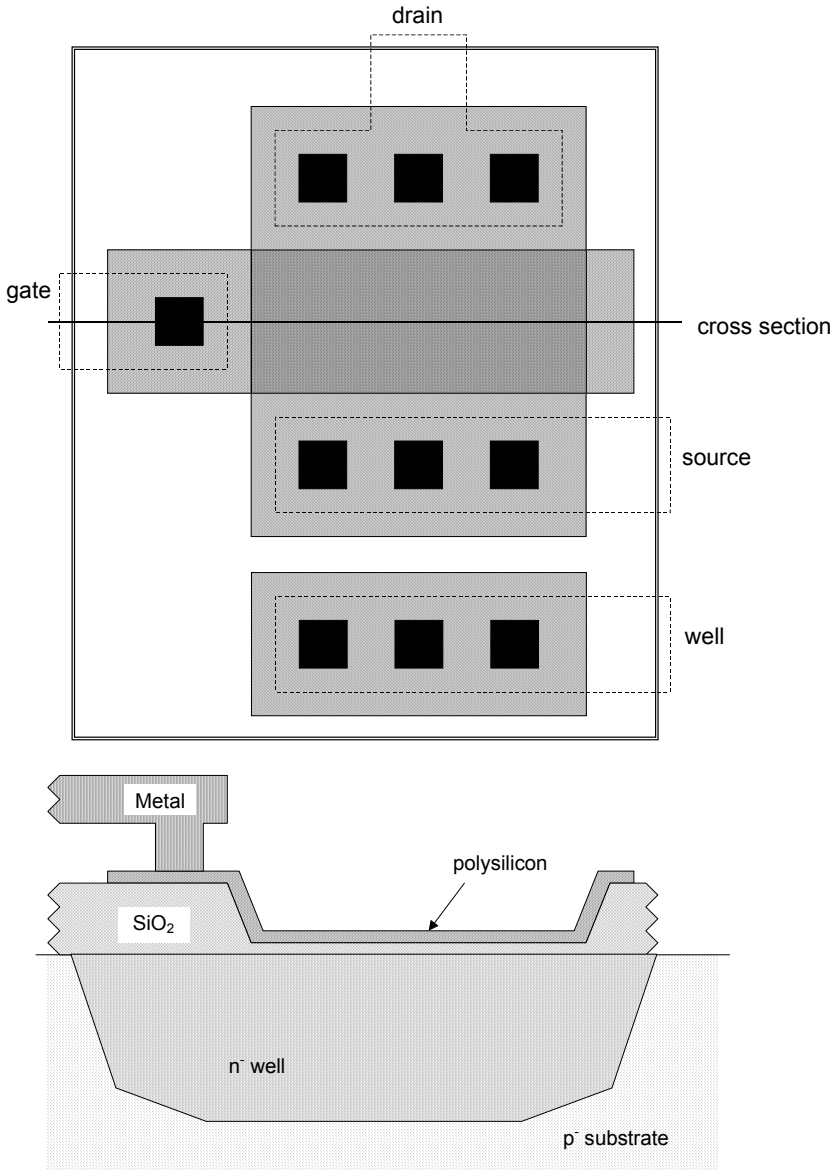
pFET Layout



- pFET requires a drawn well and a well connection
- Otherwise, identical to an nFET

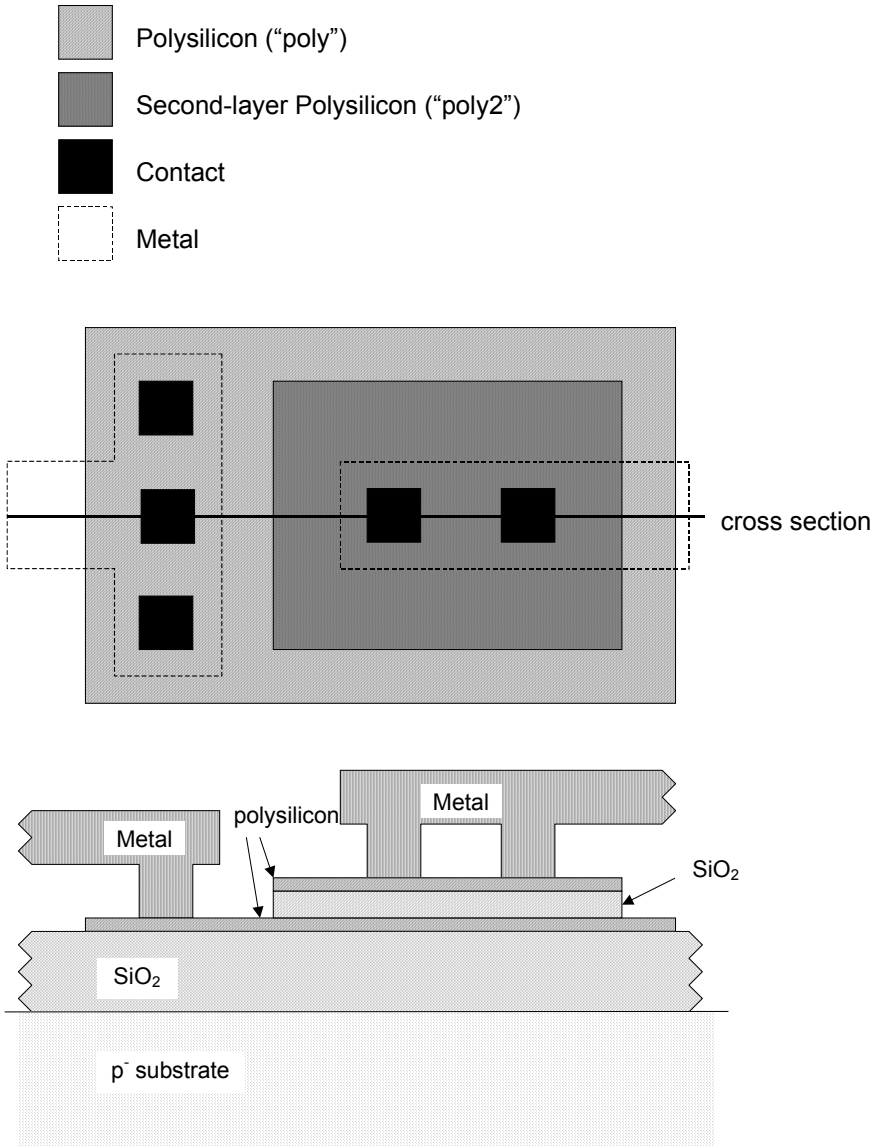
pFET Cross Sectional Views



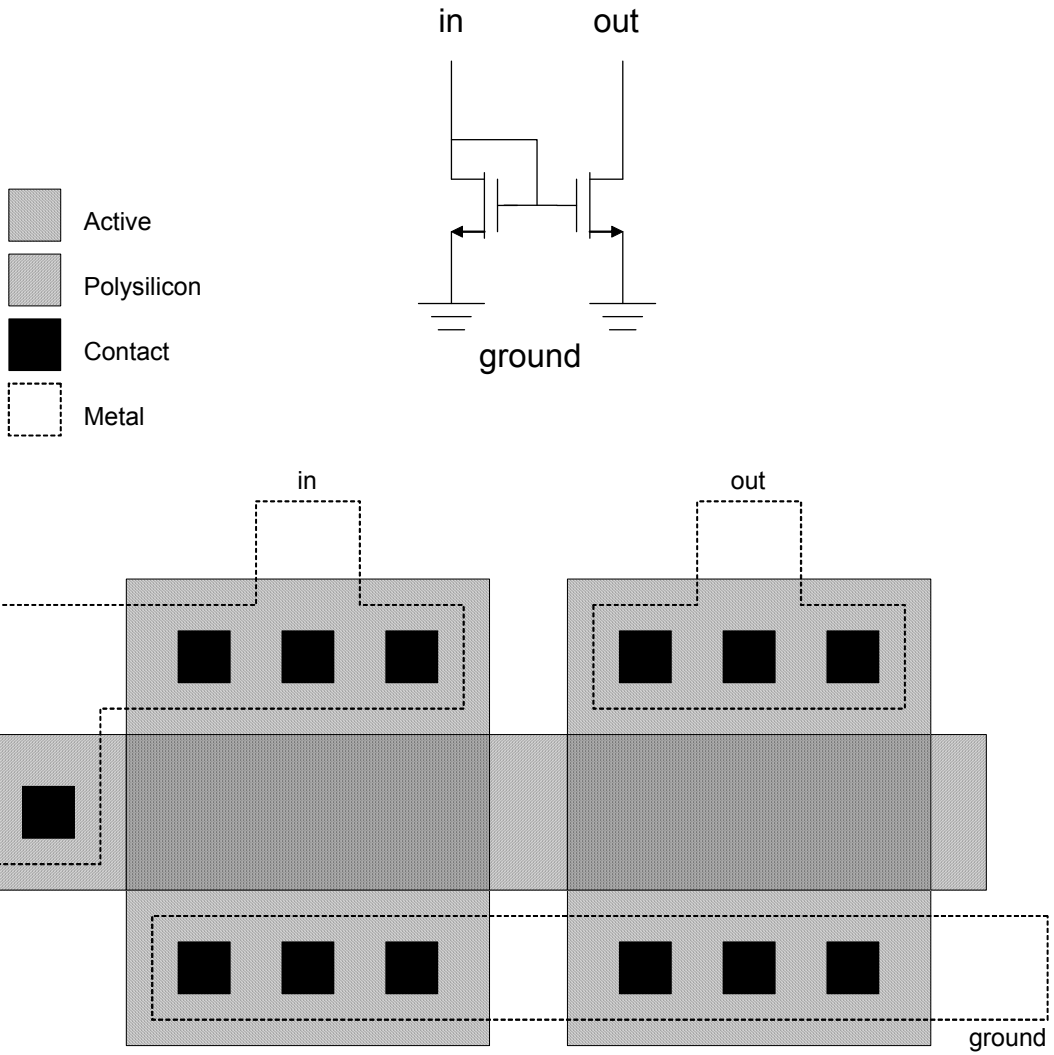


Poly-Poly Capacitors

- Some processes have two polysilicon layers for making linear capacitors.
- Typical capacitance is 0.5-0.9 fF/μm^2
- There is also a “bottom plate” capacitance between the lower poly layer and the substrate that is typically about 10% of the poly-poly2 capacitance
- If there is no poly2 layer, capacitors are made from MOSCaps

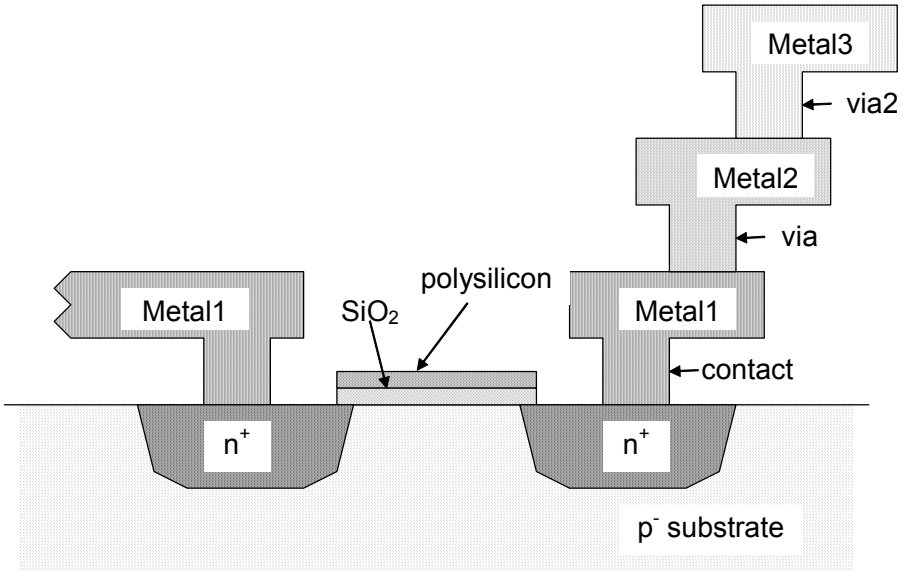


Example Layout



Multiple Metal Layers

- Contacts connect bottom-layer metal (metal1) to active (n+ or p+ regions), poly, or poly2.
- Metal2 can be connected to metal1 using a via.
- Metal3 can be connected to metal2 using a via2.
- Thus, if we want to connect metal1 to metal3, we *must* go through metal2 using a via and a via2.
- In some processes (including the one we use in this class), vias/contacts may be stacked vertically. In other processes, they must be offset from one another.
- Neither contacts nor vias should be placed over transistor gates.

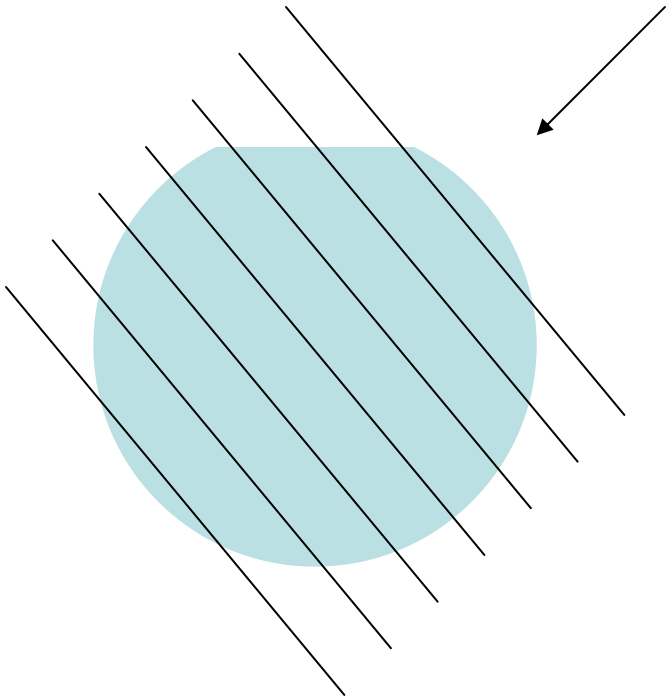


Mismatch

- One of the biggest concerns with analog layout (often “rate limiting”)
- Systematic mismatch and random mismatch
- Caused by many, many processes
  - Examples include
    - Random edge distortion
    - Corner-rounding distortion
    - On-chip concentration gradients
    - Under etching

Concentration Gradients

- Due to fabrication non-idealities, concentration gradients arise in the silicon wafer
- Systematic variation of parameters across a chip
  - Ex. gate oxide thickness, diffusion doping concentration, temperature
- Designs must be robust to concentration gradients
  - Direction of gradients are not known *a priori*

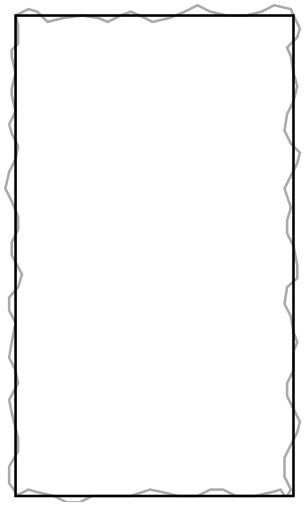


Rules of Thumb for Improved Matching

- Large Devices
- Close Proximity
- Same Orientation
- Multiple, equally sized devices
- Common-centroid layout
- Dummy elements for fringe effects
- Symmetry wherever possible

Large Sizes

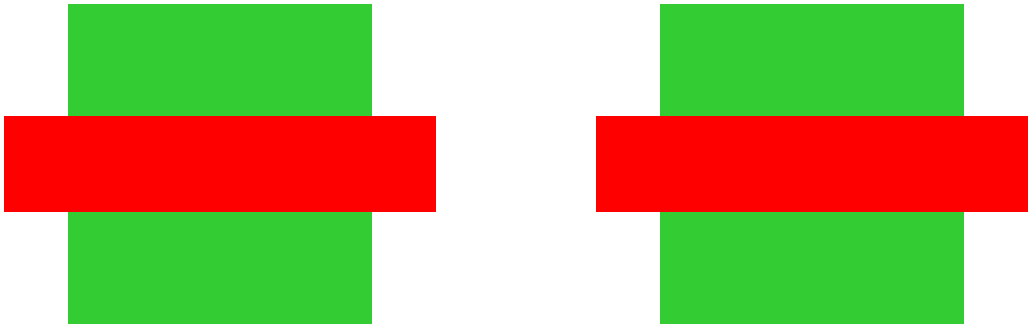
- Large sizes minimizes edge distortion
- Edge distortion can be represented by dimension + Δ
- Larger dimensions reduce the effect of edge distortion by
  - Averaging
  - Smaller contribution of Δ to overall area (important for capacitors)



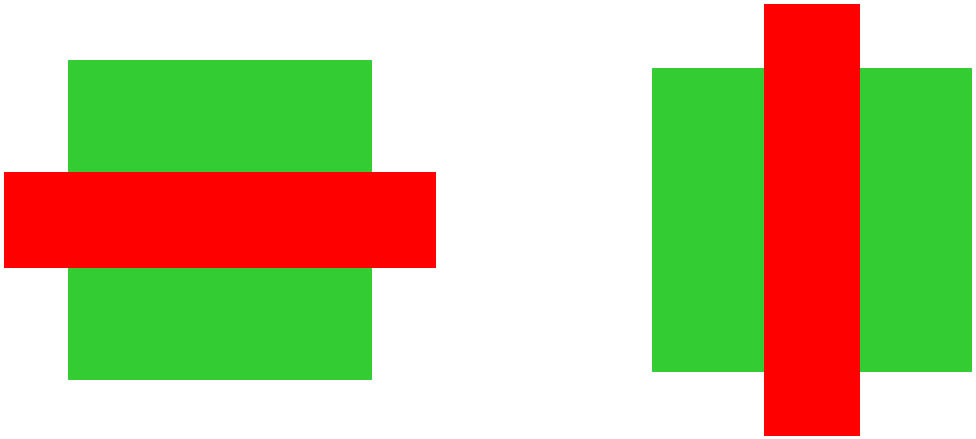
Devices with Same Orientation

- Keep matched devices close together
- Orient them in the same direction
- Current flow in the same direction

Good

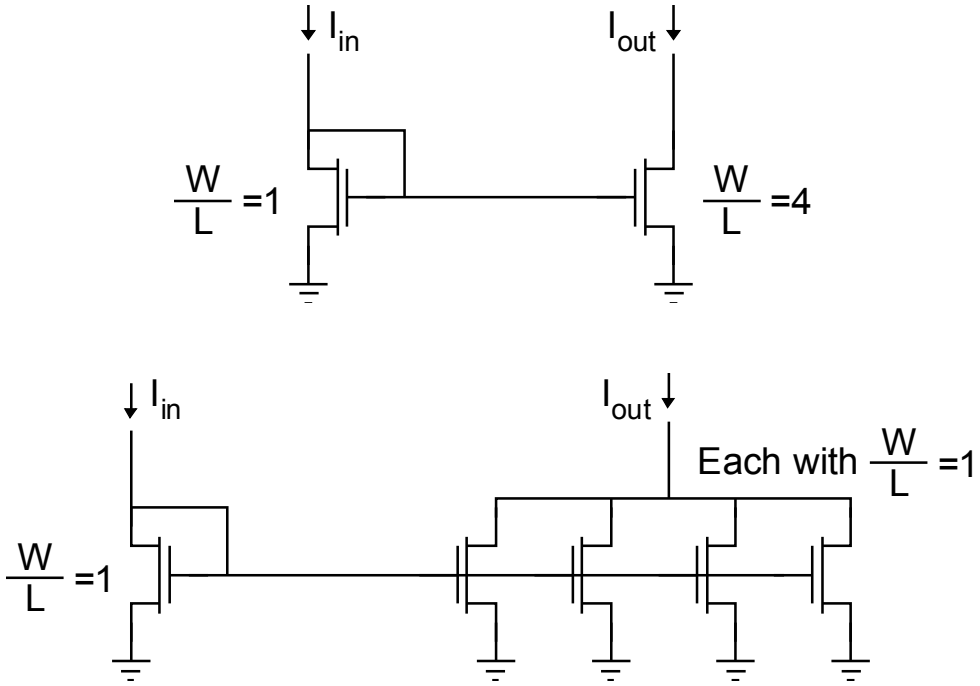


Not as good



Equally Sized Devices

- CMOS processes are relatively good at matching *ratios*, but not absolutes
- Use multiple “unit-sized” devices

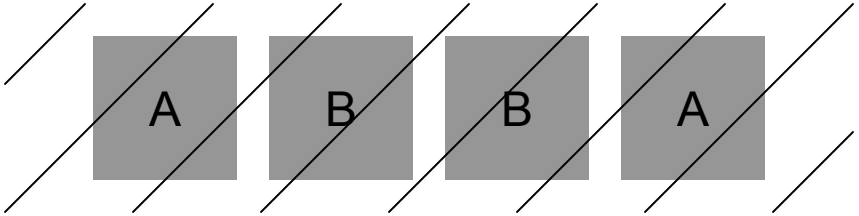


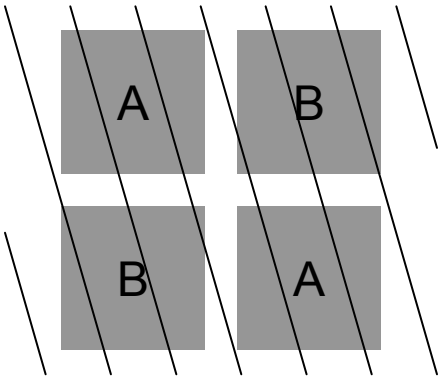
Common-Centroid Layout

- Ensure that all devices that are being matched have a “common centroid”
  - Will *remove* the effects of *linear* gradients
  - Will *help* with non-linear gradients, but not completely remove

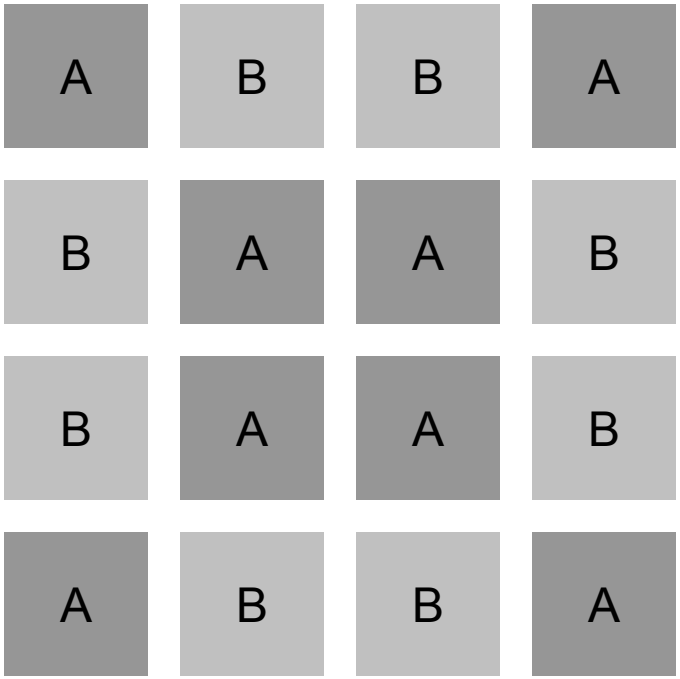
Common-Centroid Layout Examples

Let A=B. Match A and B.



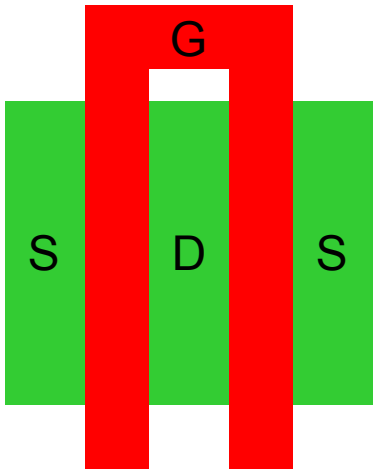


Common-Centroid Layout Examples



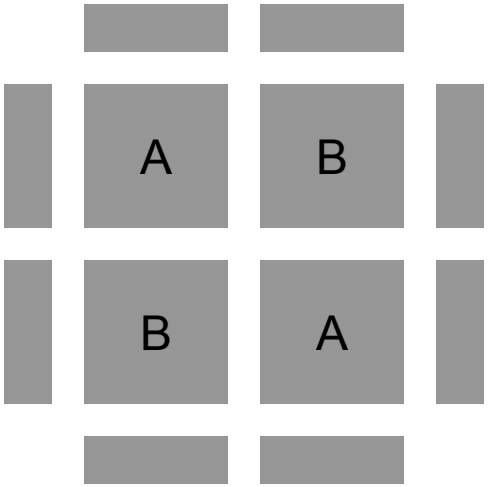
Multiple “Fingers” for Transistors

- Reduces layout to multiple, identically sized devices
- Split transistors into *M* narrow transistors in parallel (but maintain same length)
- Reduces series gate resistance (reduces noise)
- Can easily be used with common-centroid layout
- Ex. $M = 2$



Dummy Devices

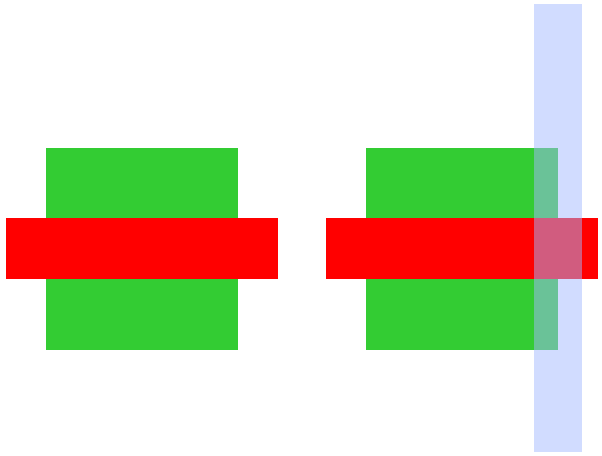
- Place “dummy” devices surrounding your devices so that they all “see” the same thing.
- Ex. Capacitors



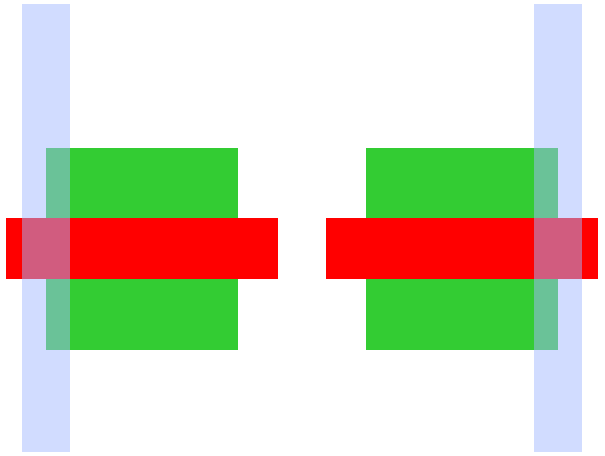
Symmetric Layout

- It helps if all devices “see” the same thing
- Example for matching two transistors

Not Symmetric

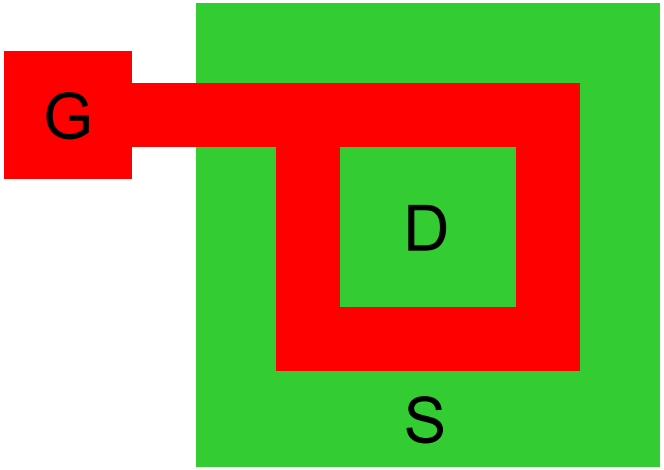


Symmetric



“Doughnut” Transistors

- Reduces
  - Gate-to-drain overlap capacitance
  - Drain-to-bulk junction capacitance
- Can improve speed of response



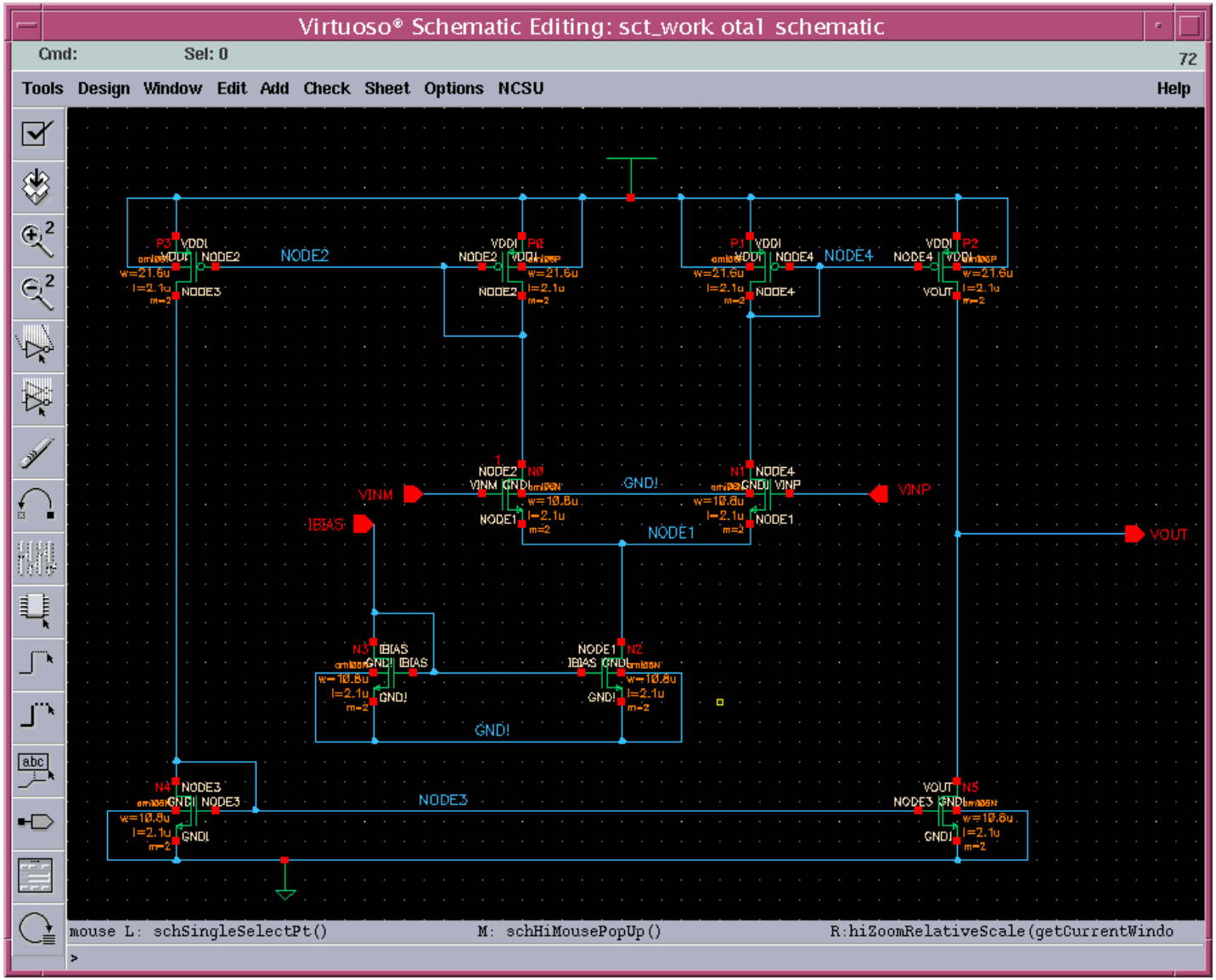
Parasitic BJTs

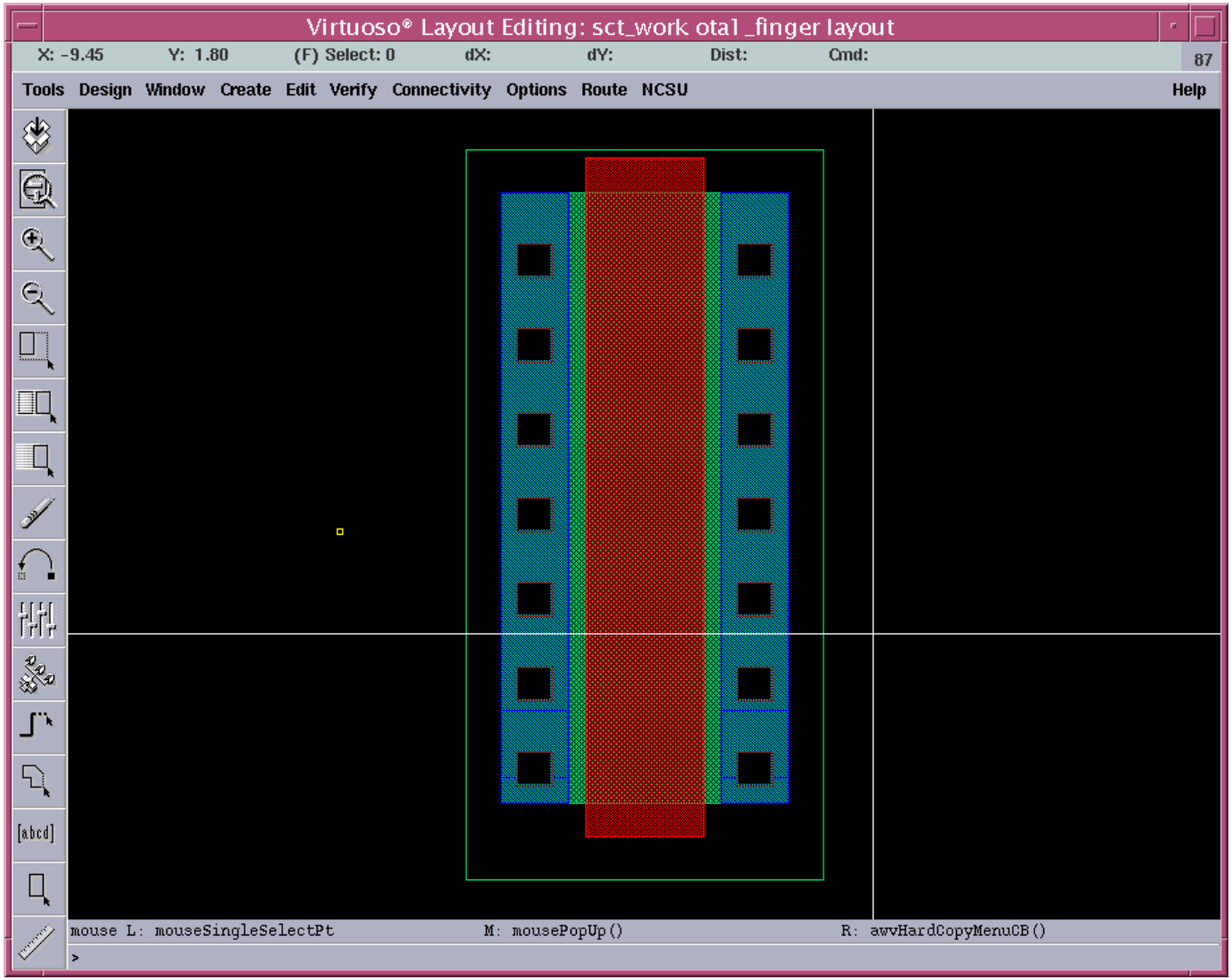
- Parasitic BJTs created by pn junctions inherent in a CMOS process
  - Substrate BJT (pnp)
    - Emitter = p+ diffusion region (within an n-well)
    - Base = n-well
    - Collector = p- substrate
    - Collector always connected to ground
  - Lateral BJT
    - Emitter = n+ diffusion region (source)
    - Base = p- substrate
    - Collector = n-well
    - Base is always connected to ground
- Sometimes purposely used
  - Temperature insenstive current sources
  - Bias currents

Latchup

- Caused by parastic BJTs within a CMOS process
- Lateral and substrate BJTs combine to form a silicon-controlled rectifier (SCR)
- Latchup typically contains two states
  - High-current state
  - Low-voltage state
- Can cause an IC to no longer work
- Can cause permanent damage
- Caused by a large current flowing over larger resistances to ground → produces a large voltage drop
- Solution → Reduce these resistances to ground
- **Use ground/well tie downs liberally!!!**

Wide-Output Range OTA




Virtuoso® Layout Editing: sct_work ota1 _finger layout
X: -9.45
Y: 1.80
(F) Select: 0
dX:
dY:
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Cmd:
87
Tools
Design
Window
Create
Edit
Verify
Connectivity
Options
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Help
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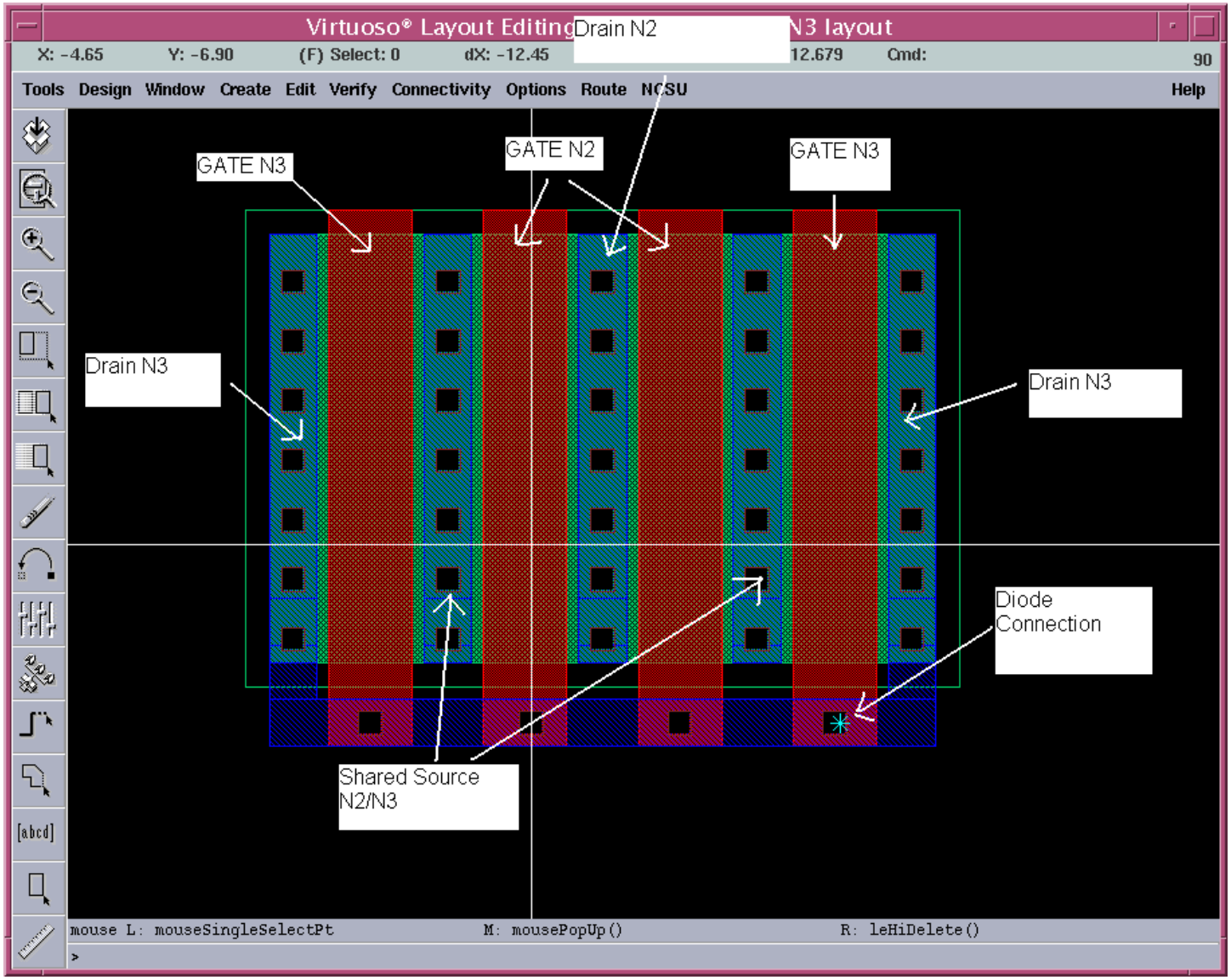
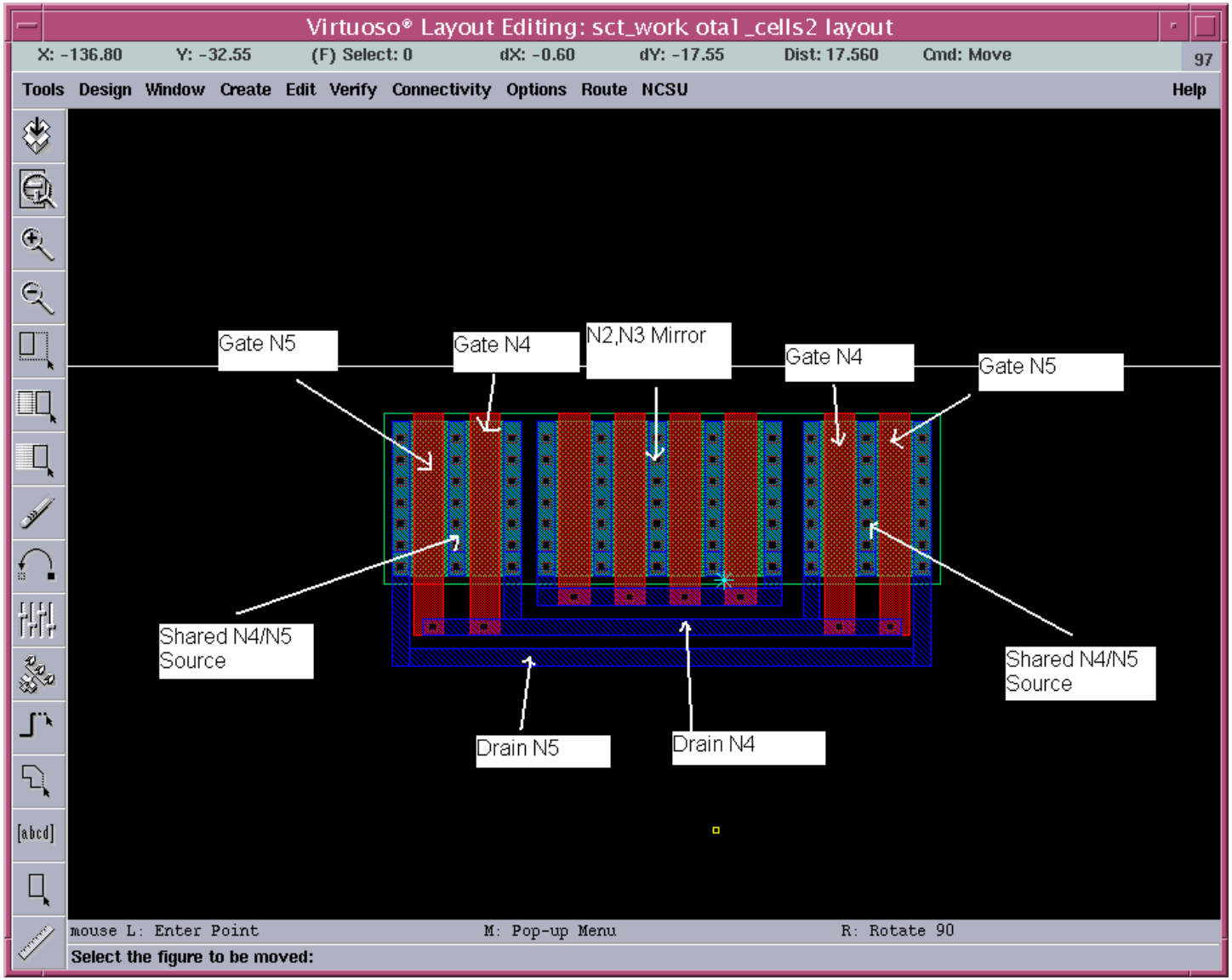
mouse L: mouseSingleSelectPt
M: mousePopUp()
R: awvHardCopyMenuCB()
>

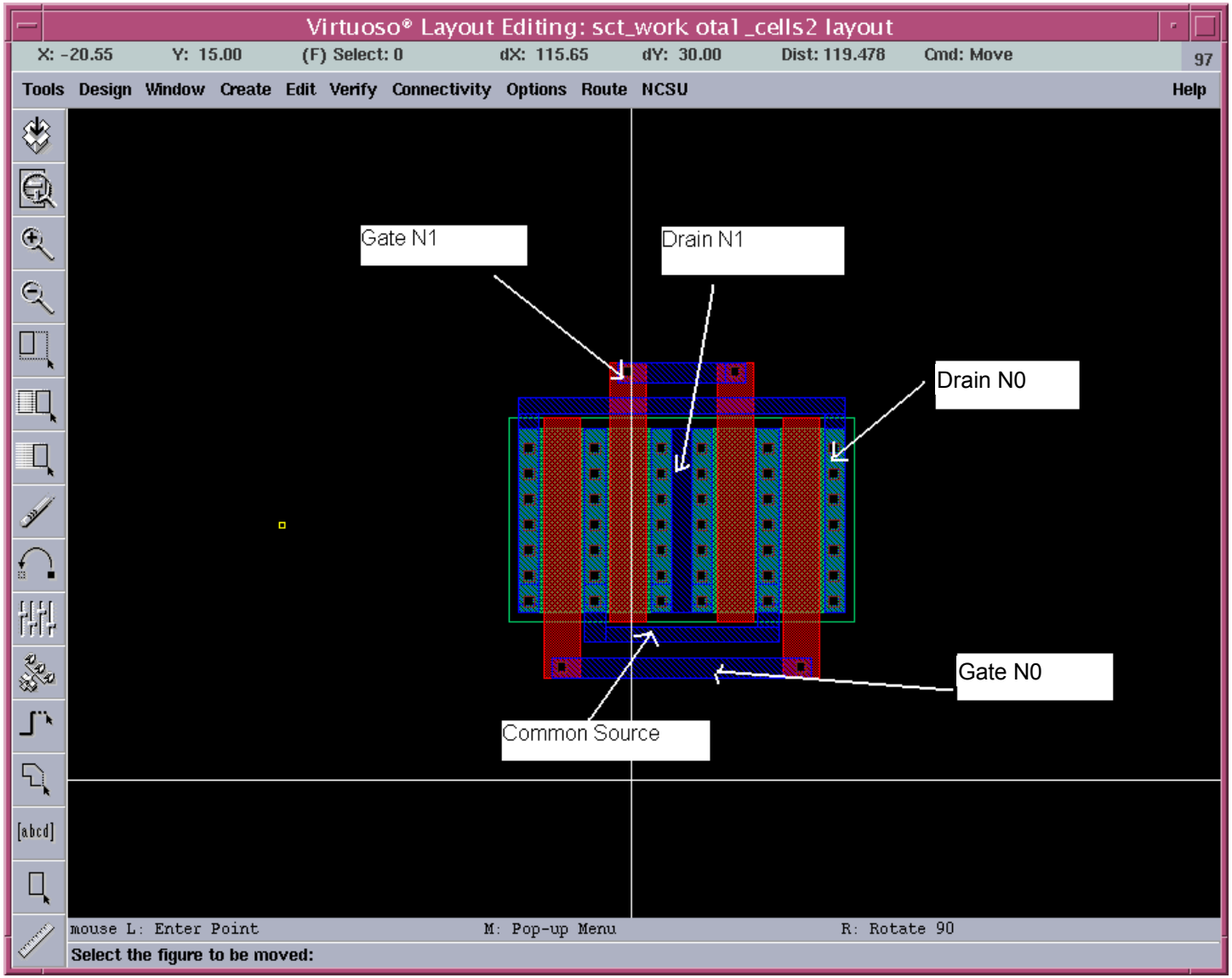
Common-Centroid Layout (Bias Current Mirror)



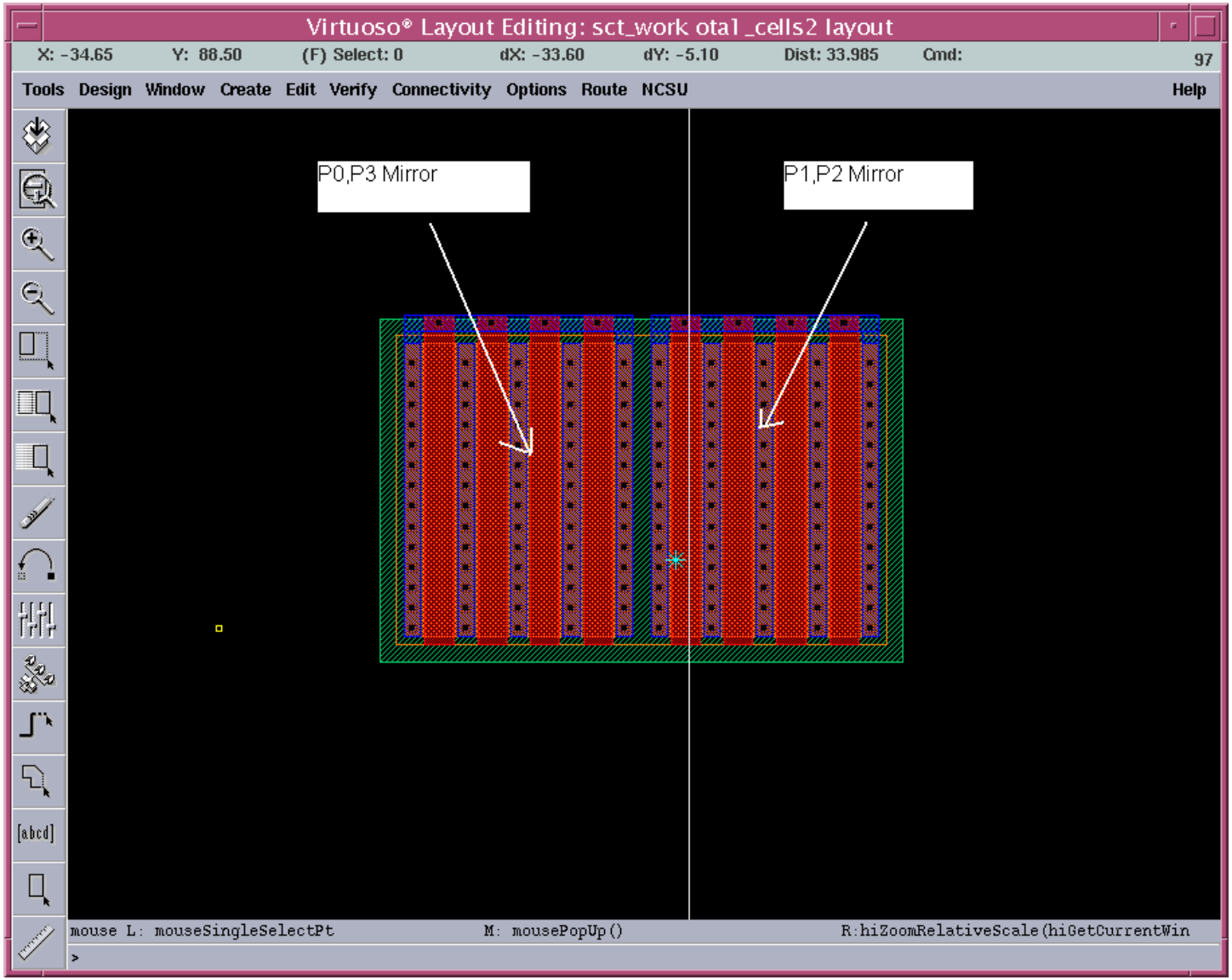
Common-Centroid Layout (2 Current Mirrors)



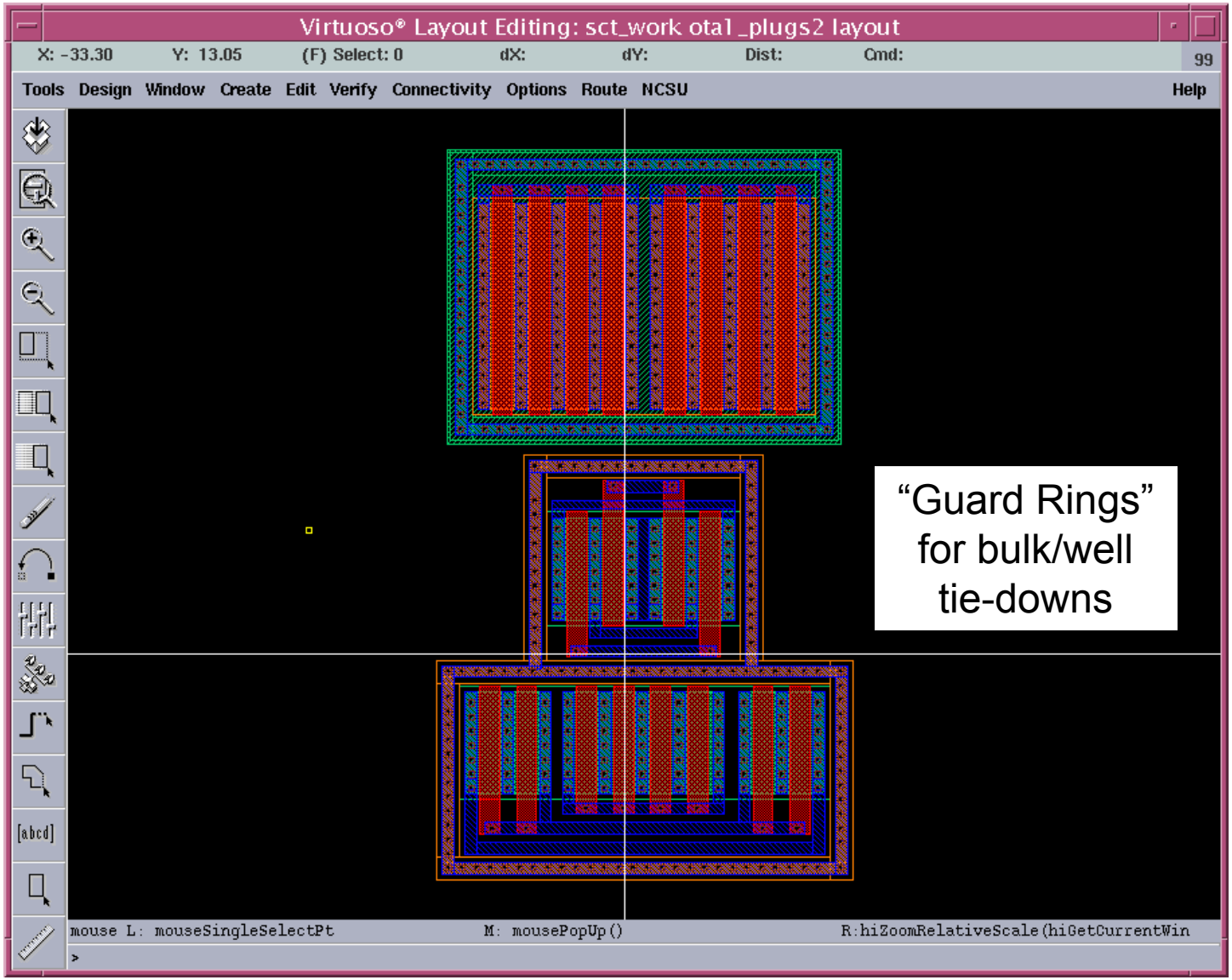
Input Pair


Virtuoso® Layout Editing: sct_work ota1_cells2 layout
X: -20.55
Y: 15.00
(F) Select: 0
dX: 115.65
dY: 30.00
Dist: 119.478
Cmd: Move
97
Tools
Design
Window
Create
Edit
Verify
Connectivity
Options
Route
NCSU
Help
Gate N1
Drain N1
Drain N0
Gate N0
Common Source
mouse L: Enter Point
M: Pop-up Menu
R: Rotate 90
Select the figure to be moved:

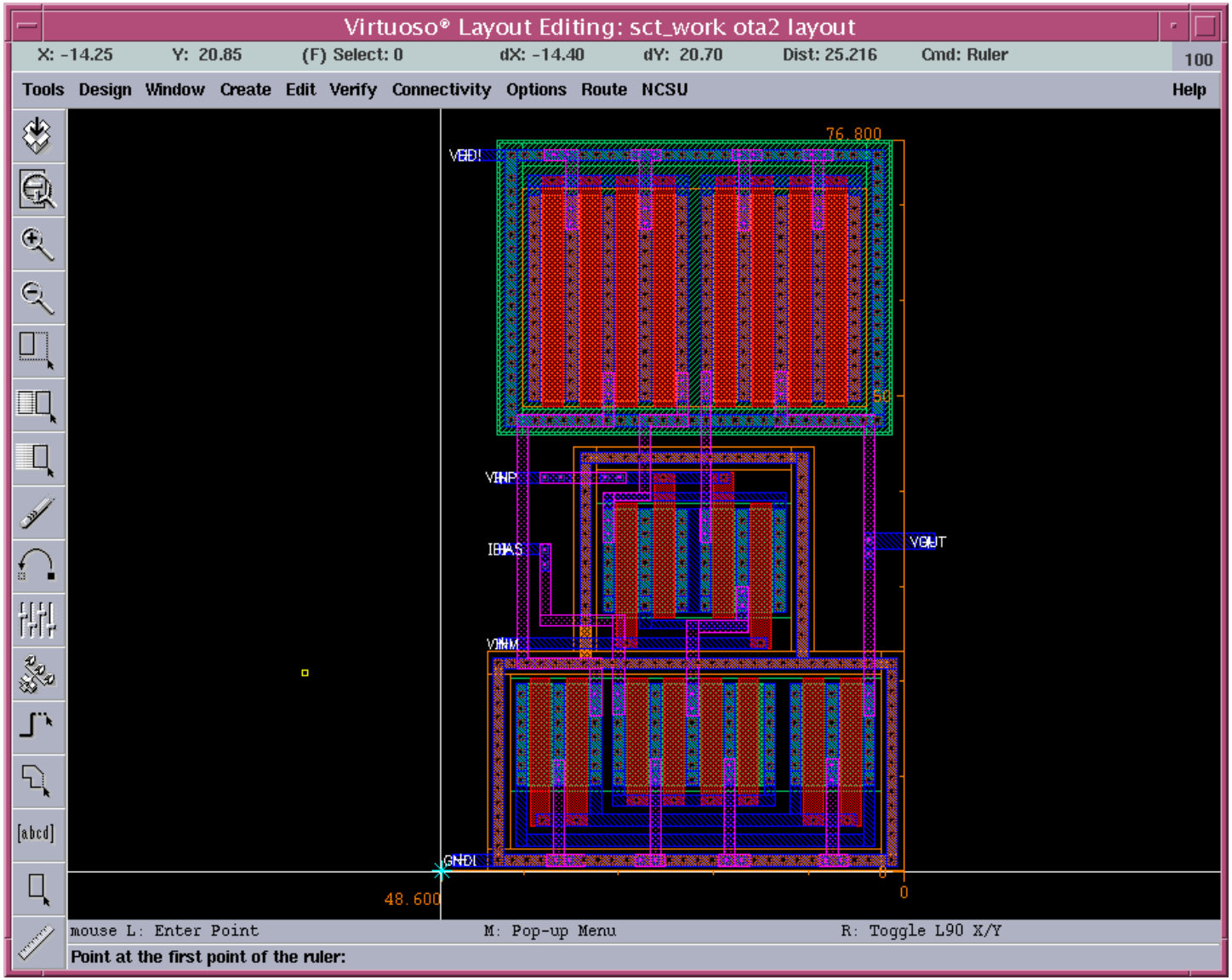
pFET Current Mirrors



All Transistors



Final Cell Layout



Analog Layout Summary

A paranoid person makes for a very good analog layout designer.