Compact and low-power continuous-time derivative circuit

A. Singireddy, K.R. McMillan and D.W. Graham

A new circuit to compute a continuous-time derivative is introduced. Comprising only one capacitor and six to eight transistors, this derivative circuit occupies very little real estate and consumes limited power, making it particularly well suited to low-power and array applications such as imager systems and sub-banded audio-processing applications. A description of the operation of this circuit is provided along with results from a circuit fabricated in a standard 0.5 μm CMOS process.

Introduction: Determining how a signal pattern varies over time is important for many perceptual and sensory processing applications. For example, temporal derivatives are used for motion detection within pixel arrays [1, 2] and for speech processing on sub-banded audio signals [3, 4]. Such applications are often implemented in continuous-time circuits to realise low-power implementations and local processing on the sensor data. In this Letter, we provide a description of the design criteria of 'frequency-normalised' continuous-time derivative circuits. We then present a novel derivative circuit that is electronically tunable and that is well suited to array-processing systems, such as the aforementioned examples, owing to its extremely compact size and low-power operation. Results are provided from a circuit fabricated in a standard 0.5 μm CMOS process.

Theoretical background: The simplest way to perform a continuous-time derivative is by using the $I = (C)(dV/dt)$ relationship of a capacitor to take the derivative of a voltage. The resulting frequency response has a magnitude with a constant slope of 20 dB/decade over all frequencies and a constant phase shift of 90°. Therefore, the steady-state response to a sinusoidal waveform is $d/dt(\sin wt) = w\cos(wt)$. Consequently, an ideal derivative emphasises high-frequency content, which limits its practical uses since the signal of interest can be overwhelmed by high-frequency noise and/or too greatly attenuated to be easily measured [1].

Therefore, a practical implementation of a continuous-time derivative circuit should operate over a limited range of frequencies. Within this band of frequencies, we can normalise the derivative with respect to a specific 'derivative frequency', ω_d, resulting in a 'frequency-normalised derivative' where

$$\frac{d}{dt}\sin\left(\frac{\omega}{\omega_d}t\right) = \frac{\omega}{\omega_d}\cos\left(\frac{\omega}{\omega_d}t\right)$$

This normalisation ensures reasonable measurements since all frequencies within the band-limited signal can be tuned to have a moderate gain (e.g. unity gain at ω_d) and since high-frequency components are filtered out due to the band-limited nature of the signal. The 20 dB/decade slope and a constant 90° phase shift of an ideal derivative must still be incorporated to provide a derivative-like operation centred on ω_d (e.g. step inputs produce instantaneous 'jumps' in the output), as opposed to merely providing a 90° phase shift. To summarise, a continuous-time frequency-normalised derivative circuit must have a tunable ω_d at which 1. the gain equals one, 2. the slope of the magnitude frequency response is 20 dB/decade, and 3. the phase is a constant 90° in the neighbouring frequencies. As a corollary to these criteria, a band-limited frequency-normalised derivative can be implemented with either a highpass or bandpass filter; if this filter has a gain >20 dB and its lowest corner frequency is $>10\omega_d$, then criteria 1–3 will be met.

Circuit implementation: Fig. 1*a* shows a schematic of our novel compact and low-power derivative circuit that is able to fulfil all of these criteria. It consists of 1. a capacitor to perform the voltage-to-current derivative, 2. a high-gain inverting amplifier constructed from a digital inverter, 3. a source follower ($M_{1\text{-}2}$), 4. a diode-connected transistor (M_3), and 5. an impedance element for feedback (M_4) commonly referred to as the Tobi element [5]. The Tobi element acts as both a very large resistive element (GΩ) for small differential voltages and also as a current limiter for larger voltages across it due to the bidirectional exponential current-voltage relationship [5].

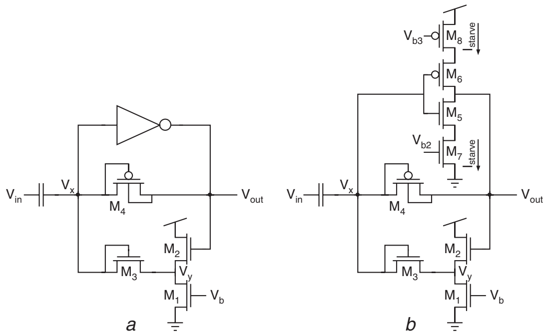

Fig. 1 *Schematics of two versions of derivative circuit*

a Standard version
b Lower-power version

The digital inverter is sized such that its threshold voltage is at approximately mid-rail. Negative feedback is accomplished through the large resistive element of M_4, which ensures that node V_x lies within the linear range of the inverting amplifier and, accordingly, maintains a nearly constant value. The source follower of $M_{1\text{-}2}$ acts as a DC level shifter so that node V_y is less than V_{out} by an amount that is dependent upon the bias voltage, V_b. As a result, there will always be a bias-dependent voltage across the diode-connected M_3, generating a current that flows out of the inverter and then through the series combination of M_4 and M_3. Linear changes in V_b produce linear changes in the offset between V_x and V_{out} which, in turn, translate into exponential changes in the current through M_3 since it operates in weak inversion. The overall transfer function of this circuit is approximately

$$H(s) = -A_v \frac{sC/(A_v(g_{m3}+g_{m4}))}{sC/(A_v(g_{m3}+g_{m4}))+1}$$

where g_{m3}, g_{m4}, and g_{Mi} are the transconductances of M_3, M_4, and the inverter, respectively, and where $A_v = (g_{m4}+g_{Mi})/g_{m4}$. This transfer function is simply an inverting first-order highpass filter, where the time constant is electronically tunable and can be established via V_b, which modulates g_{m3} and g_{m4}.

Fig. 1*b* shows a modified derivative circuit for lower-power and lower-noise operation. Here, two extra transistors are added to the digital inverter to provide current starving. Reducing I_{starve} decreases the inverter's bandwidth, which effectively reduces the highest frequency of operation of the derivative circuit. Therefore, lowering I_{starve} reduces the overall power consumption of the circuit and reduces the amount of noise that is amplified at high frequencies.

Results: Both versions of our derivative circuit were fabricated in a standard 0.5 μm CMOS process. The capacitor was implemented using a MOS capacitor to conserve chip real estate. Fig. 2 shows the frequency response of the derivative circuit of Fig. 1*a* for several biasing conditions. This circuit provides a highpass filter with a gain >20 dB and an electronically tunable lower corner frequency that is $>10\omega_d$. As a result, this circuit meets all the criteria for a frequency-normalised derivative including the 20 dB/decade slope and constant phase of −90° around ω_d (−90° instead of 90° due to inverting gain). The circuit of Fig. 1*b* provides similar results, with the exception that the upper corner frequency of the 'bandpass' filter is lowered.

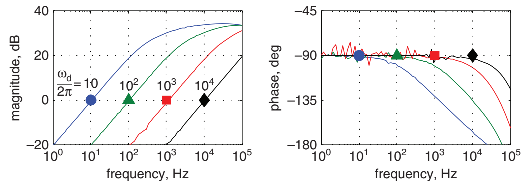

Fig. 2 *Frequency response of derivative circuit*

To demonstrate the temporal characteristics of our circuit, Fig. 3 illustrates two important test cases. In Fig. 3*a*, a step input of 10 mV was applied to illustrate the differentiation achieved when the input changes instantaneously. Accordingly, the output 'jumps' when an input step occurs and then returns to an equilibrium value when the input remains constant, as expected of a derivative operation. In the demonstration of Fig. 3*b*, we biased the circuit to perform a derivative for a signal at 1 kHz (i.e. $\omega_d = 2\pi(1\ \text{kHz})$). A 1 kHz sine wave was applied until $t = 0.01$ s, and then the input signal instantaneously transitions to a cosine at the same frequency. Fig. 3*b* shows that output of the circuit provides the negative derivative of the input with unity gain, i.e. the steady-state output for a sine-wave input is a cosine wave (with a gain of -1). The derivative circuit emphasises the discontinuities in the input signal, as expected (see $t = 0.01$ s), and quickly returns to the steady-state conditions. Results of the lower-power version of the derivative circuit (Fig. 1*b*) are identical.

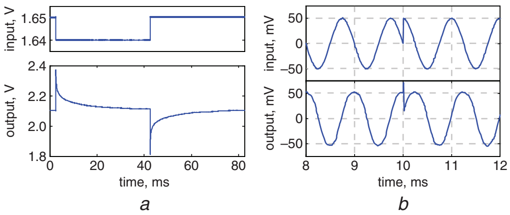

Fig. 3 *Time-domain response of derivative circuit*

a Step input and response
b Sinusoidal signal with sudden transition

Conclusion: We have outlined criteria for implementing a practical analogue derivative operation and have presented a new and compact circuit that is able to meet these criteria. Because this circuit is extremely compact (1 capacitor and 6–8 transistors) and consumes limited power (only 1.45–20.13 μW for the version of Fig. 1*b* in the audio range of 20 Hz to 20 kHz), this circuit is ideally suited for array applications. Example application scenarios include sub-band processing in low-power audio-processing systems (e.g. within silicon cochlear models [1, 6]) and motion detection in CMOS imagers [2].

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One or more of the Figures in this Letter are available in colour online.

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